Single spin devices—perpetuating Moore's law

Supriyo Bandyopadhyay

Department of Electrical and Computer Engineering & Department of Physics
Virginia Commonwealth University, Richmond, VA 23284, USA

The quest for low power

The semiconductor integrated circuits industry lives by the celebrated *Moore's law* formulated by Gordon Moore, one of the founders of Intel Corporation. This empirical law predicts doubling of transistor density on a chip every 18 months. So far, chip manufacturers have been able to keep pace with Moore's law, but recently one finds disturbing signs of stagnation. As transistor gate lengths shrink to 10 nm dimensions, excessive power dissipation per unit area is beginning to emerge as a serious spoiler. Today's transistors dissipate about 30 000–50 000 kT of energy at room temperature when they switch from one logic bit to another [1], resulting in a power dissipation of ~ 0.3 μW/transistor if the clock frequency is 2 GHz. The Pentium IV chip (introduced in 2000) has a transistor density of roughly 10^8 transistors/cm^2. Imagine now a transistor density of 10^{11} transistors/cm^2, which is what we should reach in about 15 years after the introduction of the Pentium IV chip (i.e. around the year 2015), if Moore's law continues to hold. Unless the energy dissipation in the transistor (or some equivalent device that replaces the transistor) is reduced drastically to a few tens of kT,[1] the 2015 chip will dissipate several kilowatts/cm^2 of power, thus overwhelming even the best heat sinking technology. This is the doomsday scenario that we currently face.

All this begs the question: what kind of a device can process a digital signal like a transistor and yet dissipate only a few kT of energy during switching? The answer is: one based on a single electron's spin.

All charge-based devices have a fundamental shortcoming. 'Charge' is a scalar quantity and has only magnitude. If digital bits 0 and 1 are encoded in charge (as is done in logic circuits today), then the only way we can switch between 0 and 1 is by changing the *magnitude* of this charge. This invariably causes a current flow, with an associated dissipation I^2R (I is current and R is resistance in the path of the current). Thus, charge-based electronics is intrinsically dissipative.

An electron's spin, on the other hand, is a pseudo-vector that has a 'direction' or polarization. By placing a single electron in a magnetic field, we can make the polarization bistable, since only polarizations that are parallel or anti-parallel to the magnetic field are

[1] k is Boltzmann's constant and T is absolute temperature.

Nanotechnology Perceptions **3** (2007) 159–163
Received 19 October 2007
© 2007 Collegium Basilea

eigenstates (allowed states). These two polarizations can represent the bits 0 and 1. Switching would require merely flipping the spin, *without physically moving the electron in space* and causing a current flow. This could reduce energy dissipation significantly.

Single spin logic

More than a decade ago, this thought inspired the author and his co-workers to propose the idea of single spin logic (SSL) [2]. In this paradigm, single conduction band electrons are confined in isolated quantum dots and the entire array of dots is placed in a global static magnetic field to make the spin polarization of each electron bistable. These polarizations represent the bits 0 and 1. The quantum dots are then arranged in appropriate two-dimensional patterns on a wafer. Certain dots are designated as input ports and the spins of the electrons in these dots are oriented with a local magnetic field (generated by local inductors as in magnetic random access memory chips, or spin-polarized scanning tunnelling microscope tips) to conform to the input data. These 'input dots' interact with their nearest neighbours via exchange and communicate the input data to other dots. The arrival of these input bits takes the entire system to an excited state. The system is then allowed to relax to the many-body ground state by emitting phonons, magnons, etc. By judicious arrangement of the dots, one can engineer the exchange interaction between neighbours in such a way that once the ground state is reached, the spin polarizations in certain dots, designated as output ports, always conform to the proper output in accordance with the truth table of a logic gate. Different logic gates are configured with different arrangements of the dots. The output bits can be harvested by reading the single electron spin orientations in the output dots with magnetic resonance force microscopy [3] or some other technique that is capable of single spin measurement [4, 5]. Thus, a complete logic family can be realized with interacting single spins.

Reference [2] demonstrated the working of a NAND gate. Just three electrons in three quantum dots with nearest-neighbour exchange coupling can realize a NAND gate. Agarwal [6] and Molotkov [7] have carried out rigorous quantum mechanical calculations to show that indeed if we align the spin polarizations in two of the dots to conform to either 0 or 1, then the spin polarization in the third dot automatically assumes an orientation that corresponds to the correct NAND output in response to the two inputs, as long as the system is in the ground state. This allows us to implement the NAND gate with three interacting spins. Since the NAND gate is universal, any arbitrary logic circuit can be implemented with it.

Recent advances in controlling and manipulating single electron spins in quantum dots [8–12] have brought us to the point where rudimentary SSL gates may be just around the corner. These single spin logic devices dissipate very little power when they switch (flip). In fact, the energy dissipated during the flipping of a spin is the Zeeman splitting between the two spin states, equal to $g\mu_B B$, where g is the Landé factor of the quantum dot material, μ_B is the Bohr magneton and B is the global static magnetic field's flux density. We have recently shown, using rigorous quantum mechanics, that this energy is also $kT\ln(1/p)$ where p is the gate error probability associated with a spin straying from the ground state to an excited state [6]. This dissipation—$kT\ln(1/p)$—is the minimum energy a gate must dissipate if we are restricted to an error probability p. It is known as the *Landauer-Shannon limit*. With $p = 10^{-9}$, the energy dissipated is ~ 21 kT per bit flip, which can surely allow Moore's law to be continued into the next two

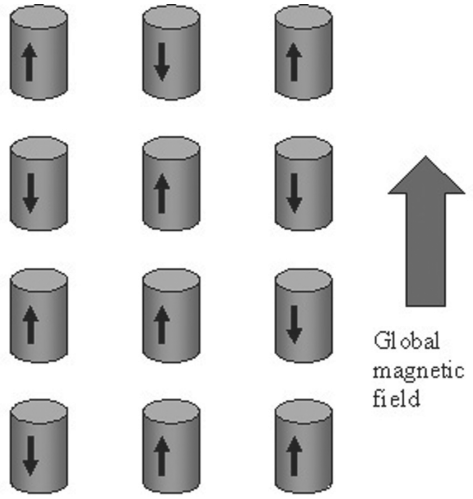

Figure 1. The NAND gate is realized with 3 spins in 3 quantum dots (shown as cylindrical dots here). The upspin state (parallel to the global field) is interpreted as logic 1 and the downspin state as logic 0. The two peripheral spins are the two inputs and the central spin is the output. Exchange interaction makes nearest neighbours have anti-parallel spins. Therefore, whenever the two inputs are both 1, the output is 0 and vice versa. When one input is 1 and the other 0, the global magnetic field resolves the tie in favour of the output being 1. This realizes NAND operation.

decades. The associated power dissipation for a 2 GHz clock is 8 pW/cell. That should allow us to achieve densities of 10^{13} bits/cm^2, if we limit power dissipation on the chip to 100 W/cm^2. Thus, the sway of Moore's law can prevail till 2025.

The issue of unidirectionality

The single spin logic family, described above, has one serious drawback that may not be obvious at first. A fundamental requirement of logic circuits is 'unidirectionality', i.e. logic signals must propagate unidirectionally from the input stage to the output stage, without back-propagation in the reverse direction. Device engineers call this feature 'isolation' between input and output terminals. A transistor intrinsically possesses isolation, but the SSL cells do not. Since exchange interaction is bidirectional, it cannot distinguish between which cell is the input cell and which is the output. In other words, the output can influence the input just as much as the input influences the output. The master-slave relation between input and output is lost.

This is a difficult problem and has been discussed in detail in a number of papers [2, 13]. It is very difficult to impose unidirectionality in space. The alternative is to impose unidirectionality *in time*. For this purpose, all cells are initially decoupled by placing a high potential barrier between neighbouring dots to make the exchange interaction negligible. Each barrier is then sequentially lowered using a clock signal. This couples the dots pairwise, one pair at a time, and ferries the logic signal unidirectionally from the input cell to the output cell in a bucket brigade fashion. A similar strategy is employed in other bucket brigade-type devices such as charge-coupled-device (CCD) shift registers, where push clocks and drop clocks are used to steer a charge packet unidirectionally from one CCD device to the next. Reference [13] showed that a single-phase clock is not adequate for this purpose; instead, a 3-phase clock is required.

Spin longevity

Earlier, we pointed out that gate errors will occur whenever a spin strays from the ground state (the correct state) into an excited state (the incorrect state). If the spin system is in thermal

equilibrium with its surroundings, then the system is governed by Fermi-Dirac statistics and the relative probability of a spin being in an excited state with energy $E_{excited}$ and in the ground state with energy E_{ground} is approximately $\exp[-(E_{excited} - E_{ground})/kT]$. We call this the intrinsic error probability p_{in}. Hence, the energy dissipated in decaying from the excited state to the ground state is $E_{excited} - E_{ground} = kT\ln(1/p_{in})$. In the 1960s, Rolf Landauer and his coworkers at IBM's T.J. Watson Laboratory showed from very fundamental principles that this is the minimum that *any* logic device (not just spin-based) must dissipate if we can tolerate an error probability no larger than p_{in}. It is now known as the Landauer-Shannon limit.

There is another source of error associated with random spin flips that occur due to external perturbations such as phonons, magnons, and spin orbit interactions. If a spin in a quantum dot flips spontaneously, then the errant spin causes a bit error. If the clock period is τ and the mean time between spin-flips is τ_s, then the bit error probability occurring during a clock cycle is $1 - \exp[-\tau/\tau_s]$. This is another kind of error and we will call this the extrinsic error probability p_{ex}. To keep this probability small, we need as large a value of τ_s as we can get. In other words, we desire materials in which the spin flip time is very long.

How long will the spin flip time have to be? Let us stipulate that we want $p_{ex} = p_{in} = 10^{-9}$. Then, if we want to work with a 2 GHz clock, so that $\tau = 0.5$ nanoseconds, we will require that $\tau_s = 0.5$ seconds. That seemed like a tall order even a year or so ago, but it no longer is. Recently, spin flip times of more than 1 second have been demonstrated in GaAs quantum dots at very low temperatures [14]. An even more striking development is the demonstration that the spin flip time in π-conjugated organic molecules can be ~ 1 second at the relatively elevated temperature of 100 K [15]. This happens because spin-orbit interactions are very weak in organic compounds, which makes τ_s long. These systems are therefore ideal for SSL-type constructs.

Conclusion

The single spin logic paradigm described here is a truly low-power architecture that can overcome some of the fundamental obstacles staring traditional charge based electronics in the face. This paradigm should be contrasted with "spin transistors" [16–20], which are really not low-power devices [21] since they are not true spin-based devices. In spin transistors, charge still plays the dominant role and logic bits are still encoded in charge stored in the active region of the device. The role of spin is a secondary one; it merely mediates the switching mechanism. Therefore, these devices do not exploit that fact that spin can be switched without moving charges physically in space and causing a current flow. Consequently, they are incapable of reducing power dissipation significantly.

Single spin devices described here may still be more than a decade away as meanwhile we begin to learn better how to control and manipulate an electron's spin in a quantum dot. However, the potential high payoff justifies serious investment in ideas of this type, and may some day return the investment in full.

References

1. The International Technology Roadmap for Semiconductors (http://www.itrs.net).
2. S. Bandyopadhyay, B. Das and A.E. Miller, Nanotechnology, **5**, 113 (2007).
3. D. Rugar, R. Budakian, H.J. Mamin and B.H. Chui, Nature (London), **430**, 329 (2004).

4. J.M. Elzerman et al., Nature (London), **430**, 431 (2004).
5. M. Xiao, I. Martin, E. Yablonovitch and H.W. Jiang, Nature (London), **430**, 435 (2004).
6. H. Agarwal, S. Pramanik and S. Bandyopadhyay, submitted for publication.
7. S.N. Molotkov and S.S. Nazin, JETP Lett., **62**, 273 (1995); Phys. Low Dimensional Struct., **10**, 85 (1997); Zh. Eksp. Teor. Fiz., **110**, 1439 (1996).
8. C. Livermore, C.H. Crouch, R.M. Westervelt, K.L. Campman and A.C. Gossard, Science, **274**, 1332 (1996).
9. T.H. Oosterkamp, T. Fujisawa, W.G. van der Wiel, K. Ishibashi, R.V. Hijman, S. Tarucha and L.P. Kouwenhoven, Nature (London), **395**, 873 (1998).
10. A. W. Holleitner, R. H. Blick, A. K. Huttel, K. Eberl and J. P. Kotthaus, Science, **297**, 70 (2001).
11. N. J. Craig, J. M. Taylor, E. A. Lester, C. M. Marcus, M. P. Hanson and A. C. Gossard, Science, **304**, 565 (2004).
12. J. R. Petta, A. C. Johnson, J. M. Taylor, E. A. Laird, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson and A. C. Gossard, Science, **309**, 2180 (2005).
13. S. Bandyopadhyay, Superlattices and Microstructures, **37**, 77 (2005).
14. S. Amasha et al., arXiv:0707 :1656.
15. S. Pramanik, C.-G. Stefanita, S. Patibandla, S. Bandyopadhyay, K. Garre, N. Harth and M. Cahay, Nature Nanotech., **2**, 216 (2007).
16. S. Datta and B. Das, Appl. Phys. Lett., **56**, 665 (1990).
17. J. Schliemann, J.C. Egues and D. Loss, Phys. Rev. Lett., **90**, 146801 (2003).
18. X. Cartoixa, D. Z.-Y. Ting and Y.-C. Chang, Appl. Phys. Lett., **83**, 1462 (2003).
19. K.C. Hall, Wayne H. Lau, K. Gundogdu. Michael E. Flatte and Thomas F. Boggess, Appl. Phys. Lett., **83**, 2937 (2003); K.C. Hall, K. Gundogdu, J.L. Hicks, A.N. Kocbay, M.E. Flatte. T.F. Boggess, K. Holabird, A. Hunter, D.H. Chow and J.J. Zink, Appl. Phys. Lett., **86**, 202114 (2005).
20. K.C. Hall and M.E. Flatte, Appl. Phys. Lett., **88**, 162503 **(**2006**).**
21. S. Bandyopadhyay and M. Cahay, Appl. Phys. Lett., **85**, 1433 (2004).