Nanotechnology Perceptions
ISSN 1660-6795
www.nano-ntp.com

VLSI Implementation of Pipelined Turbo Encoder and Decoder with Optimized Performance

Thiranambakam Deepthi Priya[1], Dr. G. Padma Priya[2]

[1]Student (M.Tech), Dept. of ECE, Sri Venkateswara College of Engineering, Tirupati
[2]Professor, Dept. of ECE, Sri Venkateswara College of Engineering, Tirupati

Systems for wireless communication make heavy use of turbo encoders and decoders. Turbo codes are used to repair network errors in 4G and 5G technologies. The present systems employ SCD (Successful Cancellation Decoder) to implement the polar codes, as opposed to LDPC and turbo coding approaches. It has reduced decoding difficulty and delay because to its short block length. The Max-Log-MAP and MAP algorithms are used for optimization in Turbo codes. The main benefit of the efficiency of this design is that the suggested approach minimizes the throughput in wireless communication systems by using a pipeline structure in boiler codes.

Keywords: LOG-MAP Algorithm, Maximum log- map algorithm, Turbo Encoder, Turbo Decoder, pipeline, convolution, RSC Encoder.

1. Introduction

Turbo encoders and decoders are essential components of modern communication systems that allow for the greatest possible data receipt with the fewest mistakes. A multiplexed code comprising two coders supplied with direct and interleaved data is produced by the encoder in the proposed Turbo System [8]. A method for error control during data transmission called forward error correction (FEC) adds redundant information to the original data so that the receiver may identify and fix faults without having to send the data again.[9]

Berrou introduced Turbo Codes (TCs) in 1993 [1].They are a type of Forward Error Correcting (FEC) code known as Parallel Concatenated Convolutional Codes (PCCC) [2]. Because they can function close to Shannon's capacity limit [3], they are used to support a number of communication standards, including Digital Video Broadcasting satellite Services to Handheld (DVB-SH), Global System for Mobile Communications (GSM), IEEE Standard P802.16, also known as Worldwide Interoperability for Microwave Access (WiMAX), and 3rd Generation Partnership Project Long Term Evolution (3GPP LTE) [4].

In order to attain the well-known Shanon limit, forward error correction, or FEC, is now a necessary technology for the design of a high performance communications system since it enables the detection and correction of faults in the sent information [5].

Turbo encoding/decoding [6] is one of the most promising methods for increasing speed [7] among all the channel coding schemes, even though the complexity rises. As a result, a number of standards use turbo encoding/decoding [8, 9, 10]. In order to improve the error correcting capacity through an iterative method, the turbo encoding concept combines two fundamental convolutional encoders, especially those based on a recursive systematic codes (RSC) architecture. By doing this, the encoder architecture no longer requires a large number of shift registers, which would greatly increase the decoding process' complexity. This enables extremely low mistake rates [7].

In [10], the effectiveness of turbo decoders and frequency-hopped spread spectrum (FH-SS) in satellite communications was assessed and contrasted with the overall effectiveness of other dynamic power allocation strategies. By altering the classical structure, a novel iterative technique for channel variance and carrier phase estimation (side information) was created, and it was shown to outperform the case where side information is unavailable [11]. A frequencyhopping packet radio structure that included turbo trellis coded modulation and continuous phase modulation was used to significantly reduce the error probability [12]. Another interesting characteristic of error correction algorithms based on more modern techniques, such as Turbo-Hadamard coding systems, is high throughput [13]. However, none of these algorithms have been verified in direct hardware implementation yet; that is, it is still difficult to incorporate them directly into a circuit description language such as VHDL or Verliog without the need for additional components like a microprocessor or Universal Software Radio Peripheral (USRP), which enables the software implementation of specific algorithmic components. In order to obtain the standardsrecommended speeds, it is common practice when using a turbo decoder scheme to try to avoid adding additional blocks than those used in traditional techniques [14], which involve the RSCs, an interleave, and a chopping block in certain cases.

In order to maximise spectrum efficiency and make effective use of capacity, the Altera® 3GPP

LTE Turbo Reference Design in [15] recommends common parameters, such as seeking the best feasible combinations of coding rates and frame lengths.

The data needed for this task was acquired in order to increase the efficiency of encoding and decoding. They were able to fix more issues with one encoder and some with the other by using two convolutional codes for the encoder. As a result, it can be corrected faster. MAP, Log-MAP, and Max-Log MAP are only a few of the many algorithms that are utilised for decoding; the decoding process goes into depth about the higher performance of Max-Log-MAP.

Comparable results are also obtained using the Viterbi technique. But in this instance, decoding was done using the Max-Log-MAP approach. The decoder will also benefit from the installation of Trellis. It is easy to spot the errors and correct them during repeated decoding because the problem location is shown here. After a specific number of iterations,

the correct result can be generated.

The pipelined components of the whole decoder assembly and the connections between its integrated components are displayed in the suggested design from [18]. The Verilog code that corresponds to the waveforms that the suggested circuit would produce also displays comprehensive simulation data, validating the final bits that were reached following the challenging decision-making process and the probabilities established at each iteration. The MATLAB software is used for comparison and validation of these results.

2. Literature Review

A method for determining the most prevalent hidden state sequence among all stated states is the Virtebi algorithm. The likelihood of any observed sequence for every combination is determined using dynamic programming methods. Pr (observed sequence | combination of concealed states) Finding the common sequence is a possible process. Each combination's whole computation is rather expensive. It is assessed for digital communications error correction for noise. The well-known Virtebi algorithm operates on the premise of a state machine for traditional codes. The system may be modelled in a specific state by using it. The number of states is limited. In a many sequence path that can result in a certain state, there will be a survivor path that is mostly a common path.

It can explain the implementations of both software and hardware. Since conventional codes are effective at repairing damaged channels, they are typically used to fix noisy channels. Deepspace communications, dial modems, TURBO and GSM cellular, satellite communications, and 802.11 wireless LANs. Use the standard codes most of the time. This algorithm is typically used in computational linguistics, bioinformatics, speech theory, information theory, and keyword spotting. The method may produce numerable statements, but it is not more likely to do so [8]. Both the concealed and visible events must occur in the same sequence in the first step, and that sequence must resemble time. The next step is to combine the two sequences and make sure that the observed or known events closely match the true one concealed event.

3. Methodology

3.1 Turbo Encoder

The Turbo Encoder architecture is shown in the Fig.1 below. The turbo encoder is composed of convolutional encoders (RSC) and pseudorandom interleaves. LTE employs one-third of the workforce. Fast code with a pace of concatenation all at once. Two distinct sets of data are used by different RSCs. The first encoder receives the original data, while the second encoder receives the interleaved data from the first data entry. One method that jumbles the data is interleaving. a notable impact on the interleaving method's performance of a decoder. Both the systematic input and the outputs from the RSC1 and RSC2 encoders consist of eight bits. The 8-bit output of the turbo encoder is produced by combining systematic input with the outputs of the RSC1 and RSC2 encoders. This is going to be sent to the Turbo decoder via the channel.

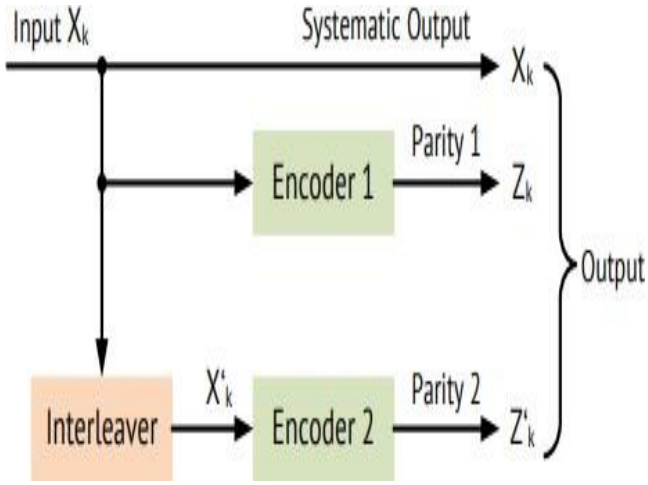

Fig.1 Turbo Encoder

3.2 Recursive Systematic Convolutional (RSC)

Encoder

Non-recursive nonsystematic (conventional) convolutional encoders can be transformed into recursive systematic convolutional (RSC) encoders by feeding back one of its encoded outputs to its input.

3.3 Turbo Decoder

The turbo decoder at the receiver end is made up of two iterative single soft-in soft-out (SISO) decoders.

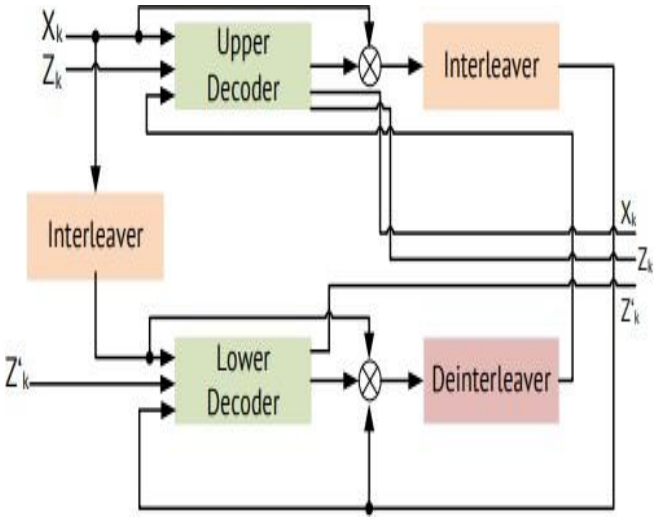

Fig.2 Turbo Decoder

When the output of the top decoder is fed into the lower decoder, as seen in Fig. 2, a turbo decoding iteration is produced. Data reordering is accomplished via interleaver and

deinterleaver blocks. Two decoding methods, LogMAP and MaxLogMAP, which are based on Maximum A Posteriori (MAP), are used for the decoding process.

Two decoders work together to form it. What drives the process is the soft decision information of each decoder. Z_k, which is known as extrinsic information, is stored as a decoder's soft choice after an operation has started. This is how the other decoder gets initialised. The decoded information is repeated until the soft decisions meet the set of values. Finally, the final extrinsic information from the first decoder is used to determine the values of the messages.

3.4 Turbo Decoding Algorithms

Iterations are the foundation of the MAP algorithm's decoding process for the turbo codes. This is used for each component code. The MAP algorithm, which is used to confirm the correctness of the incoming data, is implemented by the SISO decoder. This will get more challenging when calculating the multiplications and exponential operations needed to build the trellis diagram. Two further SISO decoders that have been developed to lower the decoder's complexity are the Max Log-MAP and Log-MAP algorithms. The MAP method is more complex than these algorithms [4].

3.5 SISO Decoder

A soft-in-soft-out (SISO) decoder's input signal is its actual (soft)value. The decoder then approximates the likelihood that each transmitted data bit is equal to one for each input bit. The turbo-decoder for the SISO component decoder that employs the maximum a-posteriori (MAP) approach is examined in this paper. The MAP technique does not restrict the set of bit estimates to precisely match a valid path across the trellis. Thus, that should not be the outcome of a Viterbi decoder that finds the most probable actual path over the trellis. The MAP approach lowers the chance of bit error by identifying the most likely bit at each trellis point using the whole sequence that was gathered.

3.6 Interleaver

The interleaver selection is a crucial component of the turbo code design. Through the use of pseudorandom data jumbling, interleavers lessen the closeness between neighbouring bits at the convolutional encoder's input. Figure 4 shows the interleaver used in both the encoder and the decoder sections. On the encoder side, it creates a long block of data while comparing the output of two SISO decoders in the decoder part and helping with error correction. Together, the pseudorandom interleaver and pseudo-random deinterleaver function.

The encoding and decoding sides both make use of the interleaver. It joins two decoders at the output, forms a long data block at the encoder end, and helps repair errors. Upon passing the encoded data through the first decoder, just a part of the errors were resolved. Any remaining errors are repaired, the procedure is repeated several times, and the interleaved output of the first decoded data is transferred to the second decoded data after the first decoder's message has been transmitted via the interleaver. The interleaver's capacity to supply random values will help supply the parity bits from every individual RSC encoder.

4. Results and Discussions

In addition to providing a brief overview of one of the best channel coding strategies, Turbo Design and Implementation of Turbo Coder for

LTE/4G/5G, this paper provides a quick analysis of the turbo encoder and decoder structure. Lower encoded bits and upper encoded bits are regularly generated by the turbo encoder side. On the decoder side, the encoded bits are input. The decoded output from the interlever is generated, and the results of the simulation are verified using manual calculations.

The wave forms of the implemented encoder are displayed in figure 3 below. The wave forms of the implemented decoder, which has two RSC decoders with interleaver and de-interleaver blocks, are displayed in figure 4 below. One decoder initially decodes the data, followed by a second decoder that decodes the data based on the input and interleaved output of the first decoder. Ultimately, the output of the second decoder is applied to the De-interleaver to get a hard decision result.

Fig. 3: Encoder output wave forms

Fig. 4: Decoder output wave forms

5. Conclusions

In addition to giving a brief examination of the encoder and MAP decoder construction, this paper offers a brief explanation of Turbo codes, one of the best channel coding algorithms. Two highly comparable Recursive Convolutional Encoders (RSC) and a pseudo-random interleaver are used to address the encoder. Every RSC operates on two independent signs. The 8-bit transmitter and receiver synthesis ensures that the very first encoder receives the incoming message. The information sent by the transmitter can be received by the decoder in the same way. Modelsim is used to run the simulation results, while Matlab software is used to validate the output.

The presentation of a structure composed of discrete elements that favours a pipeline architecture and maintains the resources that the FPGA will use as independent as possible has also increased the design's efficiency. The findings have been displayed on an integer-arithmetic simulation to facilitate the validation process. This illustrates the effectiveness of the recommended design and shows that the outcomes correspond with those of the software simulation.

References

[1] C. Berrou, A. Glavieux, and P. Thitimajshima, ‘‘Near Shannon limit errorcorrecting coding and decoding: Turbo-codes,’’ in Proc. IEEE Int. Conf Commun. (ICC), Geneva, Switzerland, vol. 2, May 1993, pp. 1064–1070.

[2] S. Benedetto and G. Montorsi, ‘‘Unveiling turbo codes: Some results on parallel concatenated coding schemes,’’ IEEE Trans. Inf. Theory, vol. 42, no. 2, pp. 409–428, Mar. 1996.
[3] C. E. Shannon, ‘‘A mathematical theory of communication,’’ Bell Syst. Tech. J., vol. 27, no. 4, pp. 623–656, Oct. 1948.
[4] Digital Video Broadcasting (DVB); Implementation guidelines for Satellite Services to Handheld devices (SH) below 3GHz, Standard ETSI EN 302 583 V1.1.0 (2008-01) 2011.
[5] C. E. Shannon, ‘‘A mathematical theory of communication,’’ Bell Syst. Tech. J., vol. 27, no. 3, pp. 379–423, Jul. 1948.
[6] C. Berrou, A. Glavieux, and P. Thitimajshima, ‘‘Near Shannon limit error correcting coding and decoding: Turbo-codes. 1,’’ in Proc. IEEE Int. Conf. Commun. (ICC), vol. 2, May 1993, pp. 1064–1070.
[7] C. Berrou and A. Glavieux, Turbo Codes. Hoboken, NJ, USA: Wiley, 2003.
[8] R. W. Hamming. Error detecting and correcting codes. Bell Sys. Tech. J. Vol. 29, pp. 147–160, 1950 18, pp. 794-807, May 2010.
[9] Sadjadpour, H. R. Sloane, N. J. A. Salehi, M. Nebe, G. Interleaver design for turbo codes, IEEE Journal on Selected Areas in Communications, Volume: 19, Issue: 5, page(s): 831-837, May 2001
[10] J. H. Kang and W. E. Stark, ‘‘Turbo codes for noncoherent FH-SS with partial band interference,’’ IEEE Trans. Commun., vol. 46, no. 11, pp. 1451–1458, Nov. 1998.
[11] H. El Gamal and E. Geraniotis, ‘‘Turbo codes with channel estimation and dynamic power allocation for anti-jam FH/SSMA,’’ in Proc. IEEE Mil.Commun. Conf. (MILCOM), vol. 1, Oct. 1998, pp. 170–175.
[12] J. H. Gass, P. J. Curry, and C. J. Langford, ‘‘An application of turbo trellis coded modulation to tactical communications,’’ in Proc. MILCOM. IEEE Mil. Commun. Conf., Oct. 1999, pp. 530–533.
[13] S. Jiang, P. W. Zhang, F. C. M. Lau, C.W. Sham, and K. Huang, ‘‘A turbo Hadamard encoder/decoder system with hundreds of Mbps throughput,’’in Proc. IEEE 10th Int. Symp. Turbo Codes Iterative Inf. Process. (ISTC), Dec. 2018, pp. 1–5.
[14] A. Louliej, Y. Jabrane, V. P. Gil Jiménez, and A. García Armada, ‘‘Practical guidelines for approaching the implementation of neural networks on FPGA for PAPR reduction in vehicular networks,’’ Sensors, vol. 19, no. 1, p. 116, Dec. 2018.
[15] Altera,"AN 505: 3GPP LTE Turbo Reference Design",AN-505-2.0,© January 2010.