Nanotechnology Perceptions
ISSN 1660-6795
www.nano-ntp.com

Static Characterization of A Proposed Noise Immune Sram Cell at the 16nm Technology Node

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This work offers a thorough study and design assessment of SRAM cells with an emphasis on key performance metrics. An overview of memory types is given at the beginning of the article, with a focus on the significance of SRAM in a range of applications. The study examines the benefits and drawbacks of several SRAM cell design topologies for 16nm technology. In addition, it looks at ways to make SRAM cells more stable and evaluates performance indicators including read, write, and hold noise margins (RSNM, WSNM, HSNM). The performance of the suggested 9T SRAM cell is compared with that of 6T, 7T, and 10T SRAM cells at each technology in a comparative analysis. With an extra inverter and an access transistor, the 9T SRAM cell exhibits superior read SNM along with strong hold and write SNM.

Keywords: SRAM Cell, RSNM, HSNM, WSNM.

1. Introduction

Modern integrated circuits depend heavily on Static Random-Access Memory (SRAM), which is used as cache memory in microprocessors, mainframe computers, engineering workstations, and portable devices. It is essential for many applications due to its fast speed and low power consumption [1, 2].

Beyond traditional computing devices, SRAM finds utility in battery-operated systems like wireless sensors and biomedical devices. In these applications, factors such as battery lifespan and power efficiency take center stage. Furthermore, multifunctional smart devices demand minimal power dissipation [3-8]. In the realm of Chip designing, where millions of transistors coexist on a single chip, minimizing surface area becomes critical [9]. Portable devices prioritize low power consumption, making it a primary consideration [10]. Arrays of SRAM cells are commonly employed to oversee substantial data loads. However, as transistor

dimensions' scale down, innovative technologies are necessary. These advancements reduce cell area and enhance integration density, but unfortunately, they also exacerbate leakage current [11-16]. Leakage remains a challenge at the individual cell level, and when multiplied across an SRAM array, it becomes a significant source of current loss. The issue of data stability in SRAM cells arises due to voltage scaling and device dimensions in emerging technology generations [17 - 19].

An SRAM array is the configuration and layout of static random access memory cells within a memory module or chip. The random-access data storage and retrieval offered by the SRAM array enables quick read and write operations. A single SRAM cell, which normally consists of six transistors, is the fundamental component of an SRAM array [20]. One bit of data can be stored in a flip-flop circuit made up of these transistors. The addressable locations of the memory are formed by aligning many SRAM cells in a grid-like layout, with rows and columns making up the SRAM array.

The block diagram for the 4x4 SRAM array in Fig. 1 shows the SRAM architecture, which is composed of an array of cells, bit lines and bit bars, word lines, sense amplifiers, and sense enable, pre-charge the circuit; data input and data out; row and column decoders; write enable WL; and so on. Here, the memory element in the array that must be written to or read from is selected using a row and column decoder. When WL write enable is 1, a read operation is conducted; when write enable is 0, a write action is conducted with appropriate control at BL and BL [4].

The noise margin is referred to as the disparity between two voltage levels, one being the lowest level of signal allowed (logic high or logic low) and the other being the highest noise level that can be admitted without the circuit not operating optimally. It is a critical factor that decides how robust and reliable digital circuits can be under conditions of noise as well as process variations.

Static noise margin (SNM) in SRAM is used as a measure for detecting noise that can affect the stability of a memory cell. Each of these cells is a flip-flop made up of cross-coupled inverters. The SNM is determined by comparing the voltage levels that cause the cell to flip between its stable states (0 and 1). A higher value indicates better immunity against disturbances, which results in more reliable SRAM cells. Designers therefore try to make SNM maximum so that data stored by different bits in RAM remains intact even when exposed to noise from various sources like temperature changes or electromagnetic radiation due to process steps, but not limited to them.

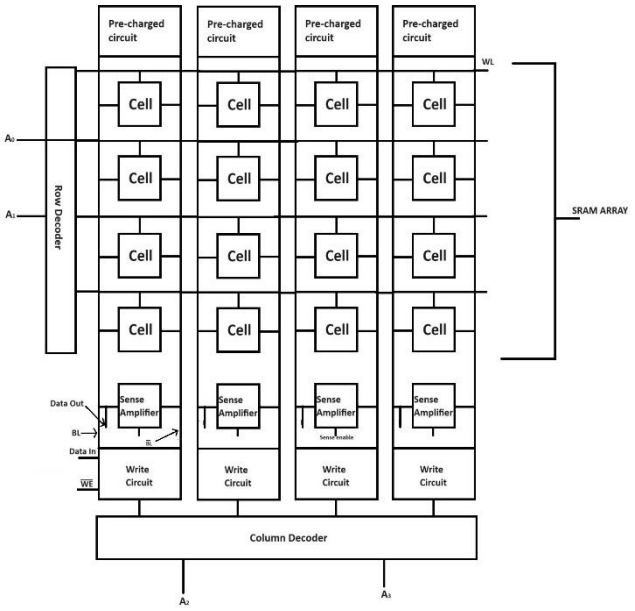

Fig. 1. Block diagram of SRAM Architecture [3]

Read SNM (Sense and Non-Sense Memory) or reading SNM refers to the ability of a memory device to accurately retrieve stored information. In the context of computer memory, it is about the capability of a memory module to accurately read the data it holds. This process involves accessing the stored information and transferring it to the processing unit or another storage medium for further use. Write SNM or Writing SNM involves the process of storing or updating data in a memory device. This process includes sending the desired information to the memory module and ensuring it is correctly stored in the designated location within the memory. Writing SNM is essential for updating information, saving new data, or modifying existing data in a memory system. HSNM, or holding SNM, refers to maintaining the integrity and stability of stored data within a memory device over time. It involves ensuring that the stored information remains unchanged and accessible for as long as required. Holding SNM is crucial for preserving data integrity and reliability, especially in long-term storage applications. This includes preventing data loss due to factors such as power failure, electromagnetic interference, or physical damage to the memory device [1-3].

Using 16nm technology and a 0.9 V supply voltage, the performance analysis and simulation of 6T, 7T, 10T, and Proposed 9T SRAM cells are done in this work on the Tanner EDA tool [25]. The RSNM, HSNM, WSNM of each of these cells are compared. Different SRAM cell architectures are explained in Section II along with associated RSNM, WSNM and HSNM simulations.

Section III compares the various SRAM cell designs. The comparison and future scope of the simulation findings are given in Section IV and V respectively.different sram cell topologies

Conventional 6T SRAM Cell

As shown in fig. 2 structure, there are a total of six transistors, with four being NMOS

transistors (specifically NM-1, NM-2, NM-3, and NM-4) and two being PMOS transistors (PM-1 and PM-2), as visually depicted in the accompanying diagram [22-25]. The configuration of this circuit comprises two cross-coupled CMOS inverters, each featuring two access transistors (NM-1 and NM-4). Data is stored within the internal nodes known as bit[v] and ~bit[v], with the assistance of an access transistor.

The operation of the cell is segmented into three distinct modes: hold mode, read mode, and write mode.

During hold mode as shown in fig. 3, the word line is rendered inactive, resulting in the deactivation of the access transistors NM-1 and NM-4. Consequently, the internal nodes, bit[v] and ~bit[v], are disconnected from the BL and BLB, respectively, preventing any alterations in the stored data. Only when the voltage supply, or WL, becomes active will changes occur in the internal nodes [21].

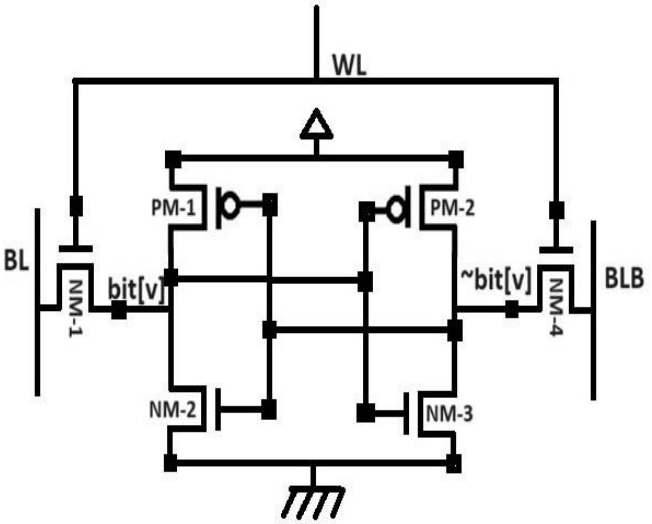

Fig.2. Schematic of conventional 6T SRAM cell [22 - 25]

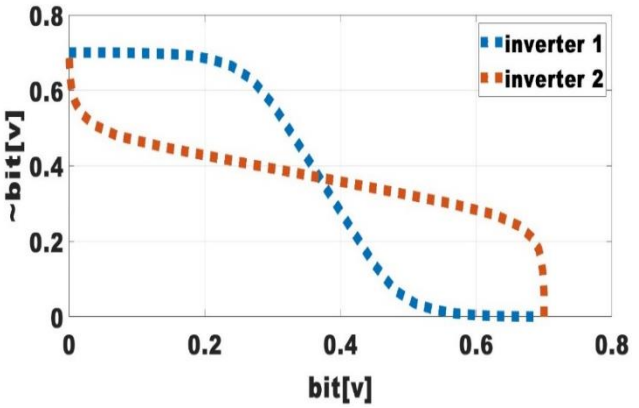

Fig. 3. HSNM at W_n=32nm, W_p=80nm

During read mode as depicted in fig. 4, BL and BLB are pre-charged while deactivating the WL. At bit [v], 0, and ~bit [v] is stored 1. In the presence of an active WL, there is no voltage discrepancy between ~bit [v] and BLB, resulting in the absence of any current flow.

However, there exists a potential difference between the internal node bit [v] and BL, resulting in a steady flow of electric current between BL and bit [v]. This discharge of current effectively diminishes the voltage level of BL, allowing the sense amplifier to sense the potential difference between BL and BLB. As a result, the sense amplifier accurately determines that a value of 0 is stored at the internal node bit [v], while ~bit [v] holds a value of 1 [21].

Fig. 5 shows the writing mode, the initial step is pre-charging the BL and BLB while disabling the WL. Assume 1 is present at bit[v] and 0 is at ~bit[v] node. Following the pre-charge of BL and BLB, the WL is then activated. If 0 is to be written at the node bit [v], where a 1 is already stored, the bit line BL on that side is set to low using an external circuit. Throughout the process, BLB remains pre-charged. The current flowing from BLB to the ~bit[v] node creates a potential difference between the two nodes, causing a flow of current from node bit[v] to BL through access transistor NM-1. As the voltage at node bit [v] decreases, the potential at node bit [v] falls below the threshold of NM-3, causing NM-3 to turn off and PM-2 to turn on. This halts the discharging at node ~bit[v], resulting in a write of 1 at node ~bit[v] and 0 at bit[v] node [21]. Table 1 gives the NM, RSNM, WSNM values of 6T at 16nm technology node.

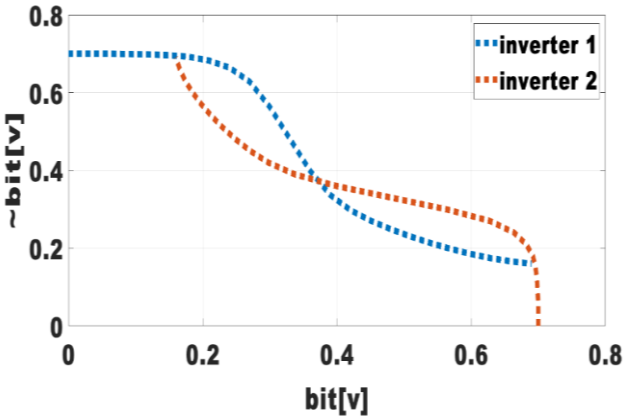

Fig. 4. RSNM at W_n=32nm, W_p=80nm

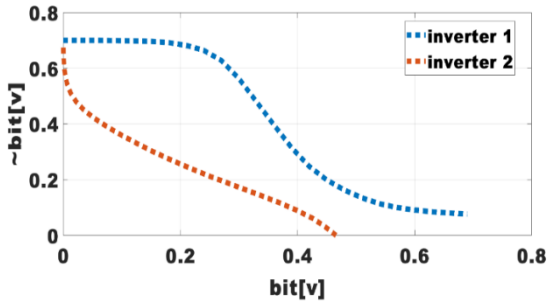

Fig. 5. WSNM at W_n=32nm, W_p=80nm

TABLE I. HSNM, RSNM, WSNM VALUES OF 6T AT 16NM TECHNOLOGY

Parameter (L_{min}=16nm, W_n (width of NMOS), W_p (width of PMOS)	Hold SNM (V)	Read SNM (V)	Write SNM (V)
W_n=W_p=32nm	0.2593	0.05939	0.3818
W_n=32nm, W_p=80nm	0.2455	0.10484	0.3177
W_n=64nm, W_p=160nm	0.247	0.0772	0.31357

7T SRAM Cell

It consists of one additional transistor in comparison to a 6T SRAM cell. This cell modal consists of five NMOS and two PMOS as shown in fig. 6. This additional transistor named as NM-2 in series with pull down transistor NM-3 and it's for the data durability in the cell [23].

As of 6T SRAM cell, the operations of cell divided into three modes- hold, read and write mode.

During the hold mode shown in fig.7, WL and WWL are inactive and WLB is active. So, the access transistor NM-1 & NM-5 gets off and there is no connection between the internal nodes and external BL and BLB. There is no change in the data stored in the internal nodes until the voltage supply or WL is active.

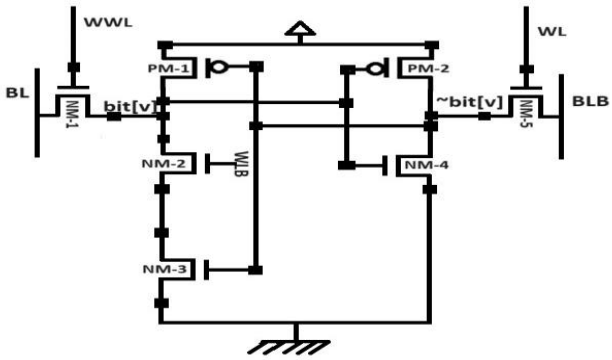

Fig. 6. Schematic of 7T SRAM cell [26]

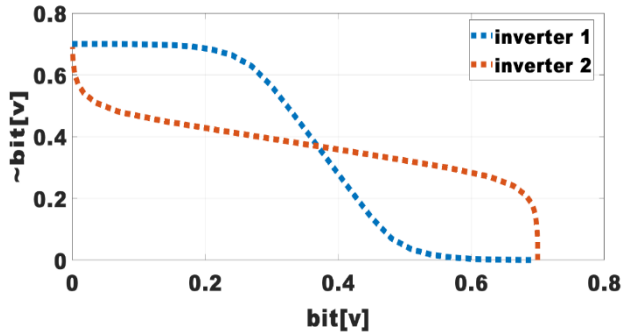

Fig 7. HSNM at W_n=32nm, W_p=80nm

As shown in fig. 8, the read operation is single sided in 7T SRAM cell. Initially the BLB is pre-charged and then WL is activated. As per the data at the node ~bit[v] there is flow of discharging current from BLB to internal node ~bit[v] through access transistor NM-5. The voltage level at BLB is sensed through external sense circuit and the value of sense voltage level estimates the stored value at internal nodes bit[v] and ~bit[v], respectively.

In fig. 9, the write mode of operation WL and WWL are enable and WLB is disabled, process remain similar with the 6T SRAM cell. while in read mode WL is active and WWL & WLB are disabled. The table 2 summarizes the simulated results.

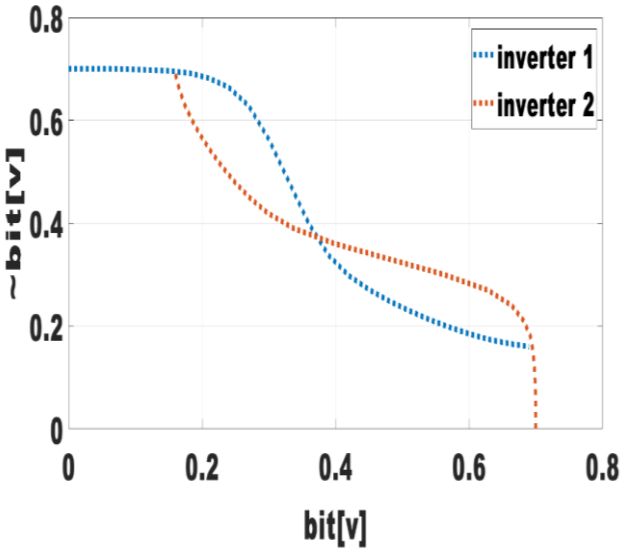

Fig. 8. RSNM at W_n=32nm, W_p=80nm

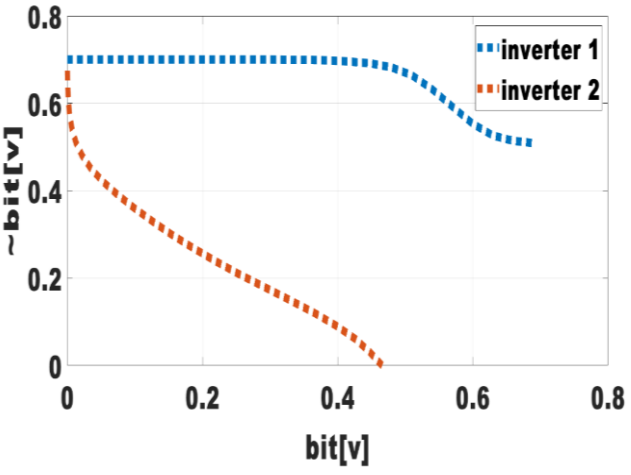

Fig. 9. WSNM at W_n=32nm, W_p=80nm

TABLE II. HSNM, RSNM AND WSNM VALUES OF 7T AT 16NM TECHNOLOGY

Parameter (L_{min}=16nm, W_n (width of NMOS), W_p (width of PMOS)	Hold SNM (V)	Read SNM (V)	Write SNM (V)
W_n=W_p=32nm	0.2593	0.0772	0.669
W_n=32nm, W_p=80nm	0.26278	0.1048	0.5138
W_n=64nm, W_p=160nm	0.2617	0.099	0.5229

10T SRAM Cell

The 10T SRAM cell shown in fig. 10 is a variant of the 6T SRAM cell and is a key component in digital integrated circuits that are designed for RAM functionality. The 10T SRAM cell, as the name suggests, has 4 additional transistors [NM-2, NM-5] and [PM-3, PM-4] as the accompanying figure implies, which takes the total number of transistors to 10. These added transistors help in enhancing stability and reducing leakage current. This provides advantages in certain applications.

In terms of operation, the 10T cell follows similar principles to the conventional 6T cell, performing read, write, and hold operations.

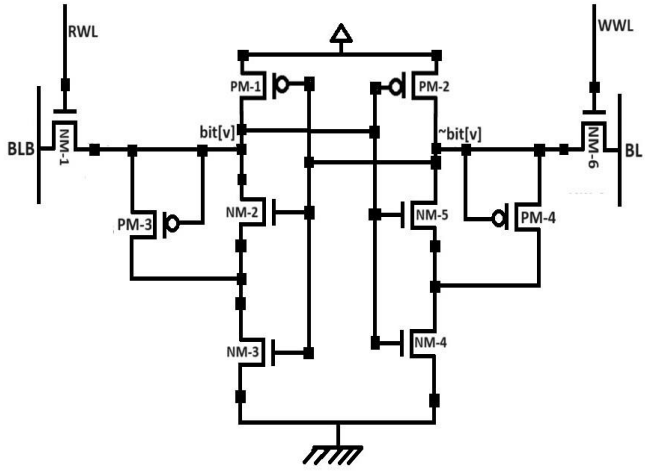

Fig.:10. Schematic of 10T SRAM cell [27]

During the HOLD operation shown in fig. 11, both word lines, RWL and WWL, are inactive, which means BL and BLB do not have any connection with the internal nodes, since the access transistors NM-1 and NM-6 are turned off. There are no changes in the data which is stored in the internal nodes until there is an external voltage supply or WL is turned ON.

In fig. 12, the READ operation involves activating one of the word lines (RWL or WWL), to enable access to the stored data. This data can be sensed through the bit lines once the word line is activated. The additional transistors in the 10T cell provide enhanced stability and reduced leakage current.

The WRITE operation in 10T is same as that in 6T as depicted in fig. 13. WL is activated in this process while the RWL remains inactive during the process. The WRITE process is initiated by selecting the word line corresponding to the target cell which enables access to

internal nodes.

The table 3 gives the simulation results using Tanner EDA.

Table III. HSNM, RSNM & WSNM values of 10T at 16nm technology

Parameter (L_{min}=16nm, W_n (width of NMOS), W_p (width of PMOS)	Hold SNM (V)	Read SNM (V)	Write SNM (V)
W_n=W_p=32nm	0.31577	0.094	0.4774
W_n=32nm, W_p=80nm	0.32546	0.14867	0.3994
W_n=64nm, W_p=160nm	0.3083	0.191	0.51997

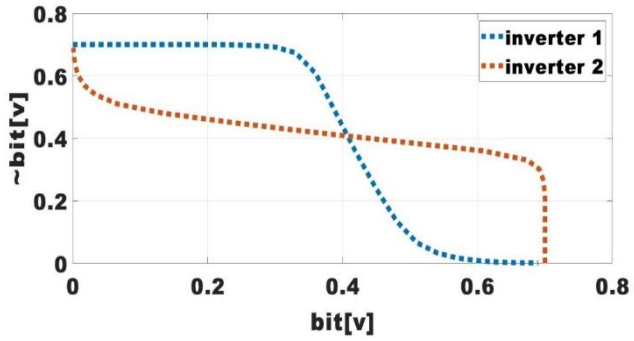

Fig. 11. HSNM at W_n=32nm, W_p=80nm

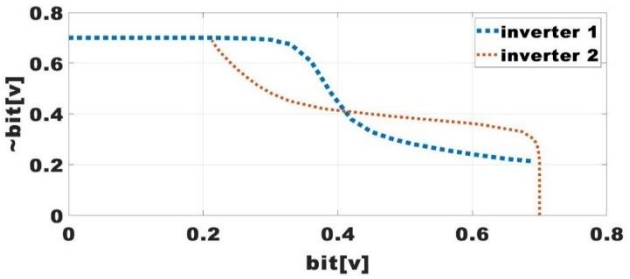

Fig. 12. RSNM at W_n=32nm, W_p=80nm

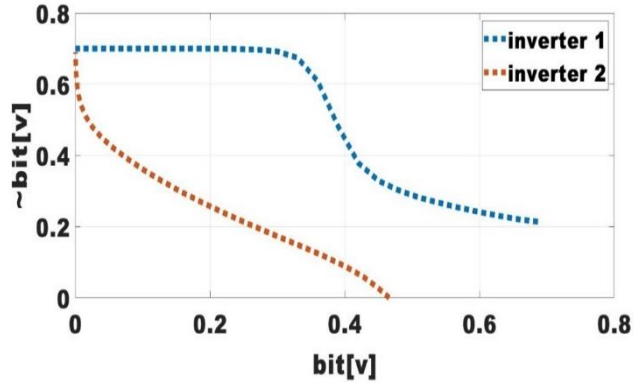

Fig.13. WSNM at W_n=32nm, W_p=80nm

Proposed 9T SRAM Cell

This circuit consists of two extra transistors as compared to 7T SRAM cell to enhance the read stability as shown in fig. 14.

While in hold mode as shown in fig. 15, WL, RWL, and WWL are disabled, and WLB is active. This causes the access transistors NM-1, NM-5, and NM-7 to turn off, preventing any connection between internal nodes and external BL and BLB. The data stored at internal nodes (bit[v] and ~bit[v]) remains unchanged, ensuring that the stored value remains the same.

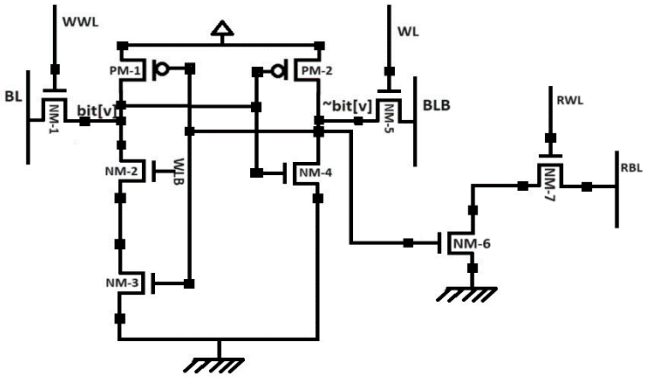

Fig. 14. Schematic of proposed 9T SRAM Cell

Only the right side of the circuit will be operational during the read operation as shown in fig.16, with WL remaining inactive. RBL is pre-charged and RWL is activated, while NM6 turns off if Q stores a '0'. As a result, there is no current flow towards NM6 from RBL, leading to no potential difference. A sense amplifier is then utilized to identify any potential variance at RBL, indicating the values stored in Q and P. If Q stores a '1', the output is reversed.

In write mode as shown in fig.17, WL and WWL are enabled, while RWL and WLB are disabled. During write operations, WL and WWL are enabled while RWL and WLB are disabled. The first step involves pre-charging the BL and BLB while disabling the WL. After pre-charging BL and BLB, WL is activated. If 0 needs to be written at bit[v], where a 1 is stored, the bit line BL on that side is lowered using an external circuit. BLB remains pre-charged throughout the process. The simulated results are presented in table 4.

TABLE IV: HSNM, RSNM & WSNM VALUES OF PROPOSED 9T AT 16NM TECHNOLOGY

Parameter (L_{min}=16nm, W_n (width of NMOS), W_p (width of PMOS)	Hold SNM (V)	Read SNM (V)	Write SNM (V)
W_n=W_p=32nm	0.25766	0.25766	0.68213
W_n=32nm, W_p=80nm	0.26019	0.2601	0.52007
W_n=64nm, W_p=160nm	0.25815	0.26126	0.52871

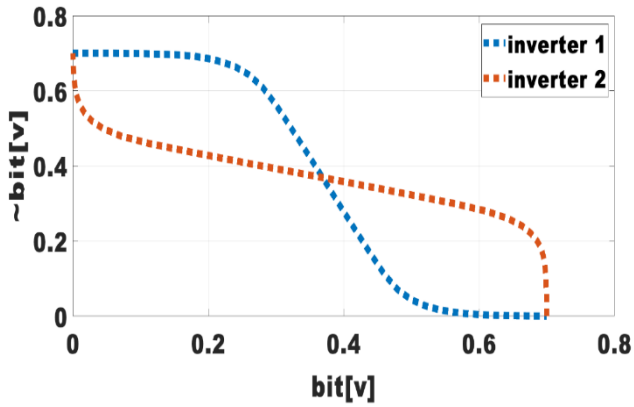

Fig. 15. HSNM at W_n=32nm, W_p=80nm

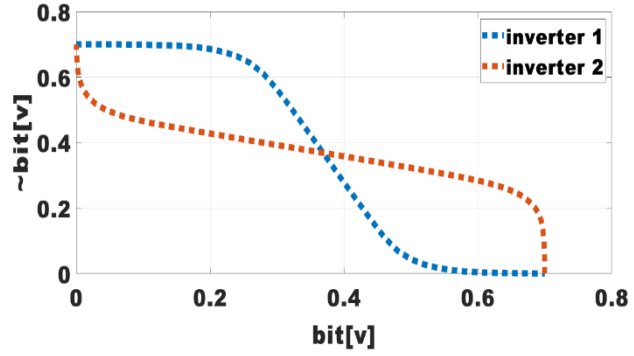

Fig. 16. RSNM at W_n=32nm, W_p=80nm

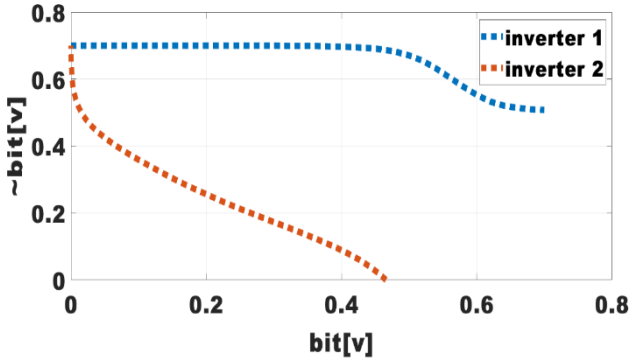

Fig. 17. WSNM at W_n=32nm, W_p=80nm

Comparison of proposed 9T against discussed topologies

This section focuses on comparing the simulation results of the discussed topologies, specifically the 6T, 7T, and 10T, with the proposed 9T SRAM cell. The comparison is based on static characteristics such as holding SNM, reading SNM, and writing SNM.

The comparison of the SRAM cells is carried out at Wn=32nm and Wp=80nm.

Figure 18 illustrates the comparison of HSNM levels among the proposed 9T SRAM cell and its counterparts, the 6T, 7T, and 10T SRAM cells, utilizing 16nm technology. The proposed SRAM cell exhibits significantly higher HSNM than the 6T cell, comparable to the 7T cell. However, the HSNM of the proposed cell falls behind the 10T cell.

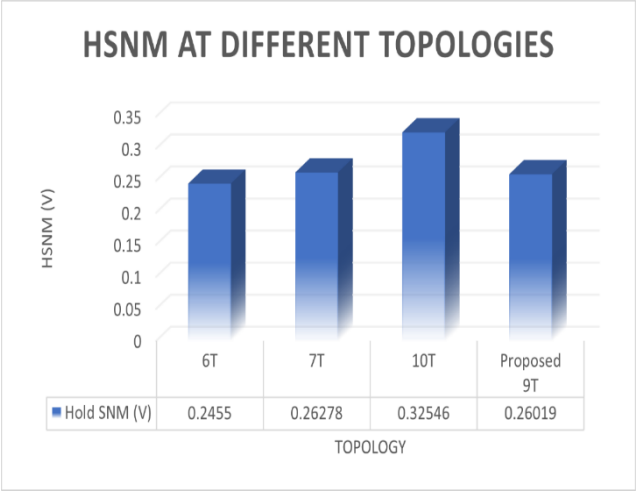

Fig. 18. Comparison of HSNM

Figure 19 displays the comparison of RSNM levels among the proposed 9T SRAM cells and its counterparts, the 6T, 7T, and 10T SRAM cells, utilizing 16nm technology. Demonstrating superior stability during read operation, the proposed SRAM cell stands out with significantly higher RSNM levels compared to its counterparts.

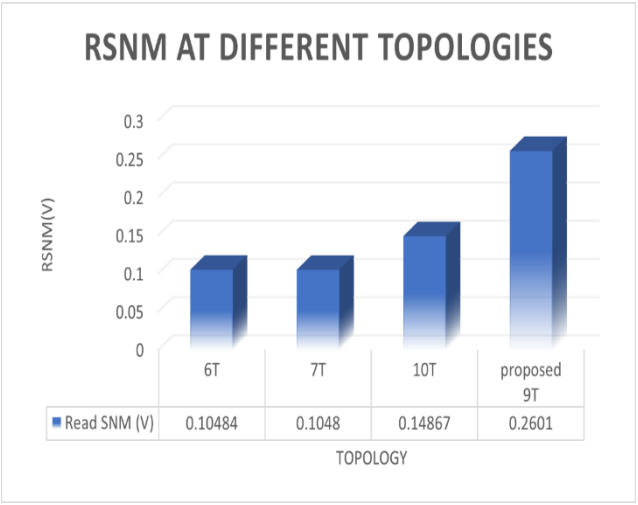

Fig. 19. Comparison of RSNM

Figure 20 illustrates the comparison of WSNM levels among the proposed 9T SRAM cells and its counterparts, the 6T, 7T, and 10T SRAM cells, utilizing 16nm technology. The findings reveal that the proposed cell exhibits notably superior WSNM compared to the 6T and 10T cells and slightly outperforms the 7T cell.

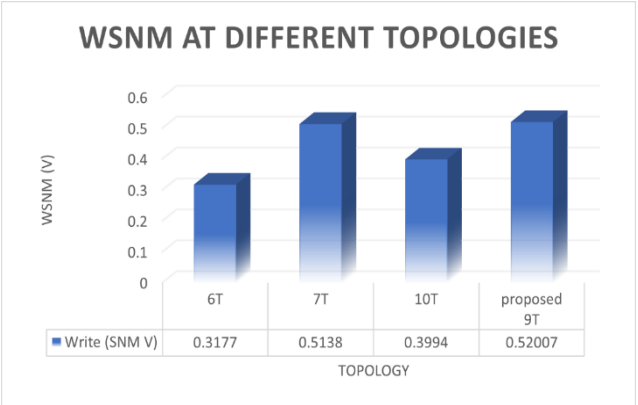

Fig. 20 Comparison of WSNM

2. Conclusion

The extensive research conducted on distinct types of SRAM cells has resulted in significant advancements and insights in the static random access memory field. This study specifically delves into the design, performance, and reliability of 9T SRAM cells, with the goal of highlighting their potential as a promising alternative to existing options. Through a thorough and methodical analysis, crucial discoveries have been made, offering valuable information for the advancement of integrated circuits.

Through the research conducted on the 9T SRAM cell, valuable insights have been gained regarding its performance in comparison to other types of SRAM cells. The 9T SRAM cell offers advantages over traditional 6T, 7T, and 10T cells, such as improved stability and reduced leakage power. One significant discovery is that the 9T SRAM cell exhibits enhanced stability during read operations, ensuring reliable performance in various conditions, and making it a promising option for high-performance and low-power applications.

The proposed 9T SRAM cell boasts a higher static noise margin, providing enhanced immunity to noise and increasing the overall reliability of memory design. This advantage is particularly valuable in today's noisy and high-frequency environments.

Future Scope

The 9T SRAM cell, comprised of 9 transistors, is a specialized variant of SRAM highly favored in the realm of high-performance integrated circuits for its exceptional stability, efficient read/write functionality, and minimal leakage current. Although forecasting precise technological developments remains a formidable task, the prospects for 9T SRAM cells are brimming with potential in various areas of advancement. The ongoing progress in semiconductor manufacturing processes holds the potential for reducing feature sizes and

increasing integration densities. This could lead to a higher number of 9T SRAM cells being packed into each chip area, ultimately expanding memory capacity.

The vulnerability of SRAM cells to instability in the form of read/write failures, retention failures, and process variations presents a significant challenge. Further exploration in research may focus on the development of design strategies or circuit-level interventions to improve stability and reliability, ultimately ensuring consistent performance in adverse circumstances. The future of 9T SRAM cells could be shaped by advancements in materials science and emerging technologies, such as nanoscale computing or alternative computing paradigms. Research into new materials and device architectures has the potential to enhance performance, decrease power consumption, and yield other beneficial characteristics. As the landscape of semiconductor fabrication technologies progresses, the potential for innovation in materials and device structures grows. The future of 9T SRAM cells lies in embracing these advancements and tailoring the design to take full advantage of the opportunities presented by emerging technologies.

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