Nanotechnology Perceptions
ISSN 1660-6795
www.nano-ntp.com

Exploring FinFET and GNRFET with a Study of Full Adder Circuit Design

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As technology keeps advancing, making devices smaller and more powerful, traditional transistors made of silicon are facing limitations. To overcome these challenges, new types of transistors are being explored, including FinFETs and GNRFETs. FinFETs are designed in 3D to improve control over electrical current and are ideal for very tiny devices. GNRFETs, made from graphene (an extremely thin material), promise better efficiency, faster speeds, and use less power due to their unique properties. This paper compares these two technologies by analyzing how they perform in circuits, specifically focusing on a commonly used circuit called the full adder. We found that while FinFETs are excellent for current needs, GNRFETs offer better energy efficiency and could be the future of electronics, especially in devices where saving power is important. The analysis highlights how each type of transistor could be applied in next-generation electronics, helping engineers design more powerful and energy-saving devices.

Keywords: FinFET, GNRFET, Nanoscale Transistors, Graphene Nanoribbons, 3D Gate Structure, Electrostatic Control, Short-Channel Effects, High Carrier Mobility, Low-Power Operation, Semiconductor Technology, Miniaturization, Device Fabrication, Advanced CMOS, Next-Generation Electronics.

1. Introduction

The electronics industry is fundamentally driven by semiconductor devices, which are integral to nearly every electronic system encountered daily. Among these devices, the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) has been a cornerstone of semiconductor technology for over forty years. Advances in MOSFET technology, such as the transition from planar to FinFET structures, have addressed challenges related to device miniaturization, operational speed, power consumption, and cost (Lone , 2021).

As transistors approach dimensions below 3 nanometers, traditional FinFETs face difficulties with gate controllability and leakage currents. The relentless drive for miniaturization in the semiconductor industry has pushed the boundaries of traditional silicon-based devices, necessitating the development of new transistor technologies. Over the past few decades, Fin Field-Effect Transistors (FinFETs) have emerged as a dominant technology, characterized by

their 3D gate structure which offers superior electrostatic control and mitigates short-channel effects. This innovation has made FinFETs particularly suitable for technology nodes below 10 nm. However, as the demand for even smaller and more efficient devices continues to grow, the limitations of silicon-based transistors become more pronounced(Kumar , 2021). Enter Graphene Nanoribbon Field-Effect Transistors (GNRFETs), which leverage the extraordinary electrical properties of graphene. Graphene nanoribbons, with their high carrier mobility and tunable bandgaps, present a promising alternative for achieving high-speed operation and energy efficiency. Despite their potential, GNRFETs face significant challenges in material fabrication and integration into existing semiconductor processes. This paper provides a comprehensive survey of both FinFET and GNRFET technologies. It examines their fundamental principles, design methodologies, fabrication techniques, and diverse applications. By comparing the advantages and limitations of each technology, this survey aims to shed light on the evolving landscape of nanoscale transistors and offer guidance for future research and development in this critical area of semiconductor technology. The motivation behind this survey paper stems from the urgent need to overcome the limitations of current silicon-based transistors, which are increasingly challenged by the demands of miniaturization and efficiency. As technology nodes shrink below 10 nm, traditional planar and FinFET transistors face significant hurdles in terms of electrostatic control, leakage currents, and power consumption. Graphene Nanoribbon Field-Effect Transistors (GNRFETs) have emerged as a promising alternative due to their exceptional electrical properties and scalability (Saha, 2018). This paper aims to contribute to the field by providing a detailed comparative analysis of FinFETs and GNRFETs, exploring their fundamental principles, design methodologies, and fabrication techniques. Additionally, it highlights recent advancements and potential applications of technologies, addressing the challenges they face and offering insights into future research directions. By doing so, this survey seeks to guide researchers and industry professionals in developing the next generation of high-performance, low-power transistors. The growing demand for smaller, faster, and more energy-efficient electronics has pushed traditional silicon-based transistors to their limits. To keep up with this demand, new technologies like FinFETs and GNRFETs are being developed. This paper aims to understand how these advanced transistors perform and which one holds more potential for the future of electronics. This study provides a side-by-side comparison of FinFETs and GNRFETs by evaluating their performance in a full adder circuit, which is a basic building block of many digital systems. It offers insights into the strengths and weaknesses of both technologies, showing that GNRFETs may be better suited for future low-power, high-performance devices, while FinFETs continue to excel in current applications.

2. Background Studies

FinFET Technology

A FinFET technology, introduced to address the limitations of planar MOSFETs, features a three-dimensional fin-like structure that enhances gate control, reduces leakage, and improves both performance and power efficiency. This technology has been widely adopted, particularly in mobile devices, due to its superior performance compared to traditional planar transistors. The evolution of FinFET began with the DELTA structure in 1989 and the double gate SOI

MOSFET in 1992, with significant advancements made by Dr. Chenming Hu in 1999. Key improvements include the use of strained Si and SiGe channels for increased carrier mobility and the implementation of high-k dielectrics like HfO2 to address tunneling issues. FinFETs offer better performance, higher frequency response, and improved thermodynamic stability, making them a crucial technology for advanced semiconductor applications(Priyanka, Singh, S.K ,2019).

Evolution and Innovations in FinFET Technology

The next phase of FinFET evolution involves various innovative structures aimed at enhancing device performance. In 2005, a double gate (DG) FinFET with a gate-source/drain underlap region was designed to optimize source/drain resistances. In 2007, a triple gate FinFET reduced gate tunneling current and improved performance, while high-k dielectric materials improved short channel parameters. In 2009, corner effects in triple-gate bulk FinFETs were suppressed by increasing body doping at the corners. In 2014, a High K/Metal Gate (HKMG) FinFET architecture optimized electrostatic behavior by varying Fin width. A symmetric high-k spacer hybrid FinFET, proposed in 2015, demonstrated superior drain current performance and mitigated short-channel effects. Various proposed architectures in subsequent years addressed issues such as leakage current, short-channel effects, power consumption, and thermal efficiency using advanced materials and design techniques. Notably, innovations such as GaAs-based SOI FinFETs, bulk FinFETs with optimized equivalent oxide thickness, and wavy FinFET designs enhanced device performance and efficiency. Recent studies in 2021 compared FinFETs with GAA FETs, highlighting better electrostatic control and reduced leakage in GAA FETs, though large-scale fabrication posed challenges. Advances in junction-less accumulation mode FinFETs and the influence of dielectric materials further improved RF/analog performance and power efficiency (Priyanka, Singh, S.K, 2019).

Graphene Technology

Due to the scaling limits of silicon, researchers are exploring alternative materials for various applications. Carbon, which has similar outer-shell electron properties to silicon but different interactions and wave functions, is a major focus due to its diverse allotropes and impressive crystal structures. These carbon-based materials include graphene-based FETs, carbon nanotube FETs (CNTFETs), nanowire transistors, single-electron transistors, and Quantum Dot Cellular Automata (QCA).

1) Nanowire Transistors (NWFETs): These devices use a thin nanowire channel and are promising for scaling CMOS technology due to their non-planar geometry, which provides superior electrostatic control and high carrier mobility. Their small diameter enhances the inversion charge through quantum confinement, making them useful for biosensing and various industrial applications.

2) Carbon Nanotube FETs (CNTFETs): CNTs are cylindrical structures of graphene with either metallic or semiconducting properties depending on their chirality. They offer high current-carrying capacity, thermal stability, and mechanical strength, making them suitable for future electronics and photovoltaics. CNTFETs can be designed in various geometries to enhance their performance and efficiency.

3) Quantum Dot Cellular Automata (QCA): QCA involves a grid of cells that follow

specific rules to perform logic functions, with potential advantages in high density and low power delay. Graphene quantum dots (GQDs) are being explored for energy storage, photovoltaics, and biomedical applications due to their unique properties.

4) Graphene Nanoribbon (GNR) Transistors: Graphene, discovered in 2004, is a single layer of carbon atoms arranged in a hexagonal lattice. It has exceptional carrier mobility and thermal conductivity. When patterned into narrow strips (GNRs), it can exhibit semiconducting properties with a bandgap dependent on width. GNRs are used in both analog and digital devices (Priyanka, & Garg, A,2018).

5) Fabrication Techniques for Graphene:

a) Mechanical Cleavage: Uses adhesive tape to peel thin layers of graphite.

b) Chemical Exfoliation: Involves intercalation, reintercalation, and sonication to produce graphene.

c) Oxidation and Reduction: Synthesizes graphene oxide and reduces it to monolayers.

d) Chemical Vapor Deposition (CVD): Deposits graphene onto metal surfaces by pyrolysis of hydrocarbons.

e) Chemical Synthesis: Uses organic synthesis techniques to create graphene quantum dots.

f) Graphene Nanotomy: A process for producing width-controlled GNRs.

6) Properties of Graphene:

a) Structural: A single layer of carbon atoms in a hexagonal lattice.

b) Electronic: Exhibits high electron mobility and behaves as a massless Dirac fermion at low energies.

c) Thermal: An excellent thermal conductor with high thermal conductivity, superior to graphite and carbon nanotubes.

Graphene's unique properties make it a promising candidate for replacing silicon in future electronics, offering potential advances in speed, efficiency, and application versatility.

Fabrication of Graphene Nanoribbons (GNRs)

Graphene Nanoribbons (GNRs) are promising semiconducting materials that could potentially replace silicon-based technologies due to their ability to support high clock speeds, up to 1 THz. Various methods are used to fabricate GNRs:

1) Graphite Nanotomy: This technique involves using a sharp-edged tool to slice graphite into nano-sized blocks, which are then exfoliated to produce GNRs.

2) Chemical Separation: Multi-layered carbon nanotubes are separated using sulfuric acid (H_2SO_4) and potassium permanganate ($KMnO_4$).

3) Plasma Etching: Nanotubes are partially embedded in a polymer film and then etched to form GNRs.

4) Ion Implantation and Vacuum/Laser Annealing: These processes are applied to a silicon carbide (SiC) substrate to produce GNRs.

Types of GNRs

GNRs are essentially nano-sized strips of graphene, and their electronic properties vary based on their edge configuration (Trivedi, 2004):

1) Armchair GNRs: These can be either semiconducting or metallic, depending on their width. Armchair GNRs typically exhibit a semiconducting behavior with an energy gap that inversely relates to their width. For a 2.5-nm-wide armchair GNR, the energy gap can reach up to 0.5 eV. Scanning tunneling microscopy is often used to control the orientation of the edges of armchair GNRs.

2) Zigzag GNRs: These are metallic due to spin-polarized edges and exhibit an energy gap influenced by antiferromagnetic coupling. This behavior is attributed to edge state wave functions and spin polarization effects, leading to significant changes in their electronic and optical properties. Zigzag GNRs show localized states at the edges with unbonded orbitals near the Fermi energy, contributing to their metallic nature.

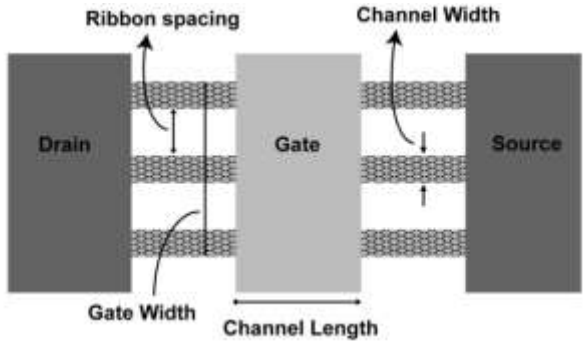
GNRs' exceptional electronic properties make them suitable for various nanoscale applications, including enhancing the mechanical properties of polymers and in biosensing technologies.

1. Graphene Nanoribbon Field-Effect Transistors Circuits

GNRFET Device Structure

GNRFET utilizes a GNR as the channel, with metallic contacts placed at the source and drain as shown in Fig.1. Graphene Nanoribbon Field-Effect Transistors (GNRFETs) are fabricated by placing a Graphene Nanoribbon (GNR) channel with metallic contacts at the source and drain (Chen, Y, 2023).

Figure 1 Graphene nanoribbon FET



It shares properties with metallic carbon nanotubes (CNTs) such as high carrier mobility, compatibility with high-k dielectrics, high carrier velocity for abrupt switching, and good thermal conductivity. While 2D graphene is a zero bandgap semimetal, a bandgap can be introduced by narrowing graphene to a few nanometers wide GNR. The edges of the ribbon, determined as armchair or zigzag by hydrogen passivation, affect the properties. Due to their

thin geometries, GNRFETs face performance issues from defects and variability's, including control over GNR width, oxide thickness, and line edge roughness during fabrication (Priyanka, Singh, S.K., & Dua, P. (2021); Chen, Y., Sangai, A ,2015).

These devices benefit from several advantageous properties similar to those of metallic carbon nanotubes (CNTs), including:

1) High Carrier Mobility: Facilitates ballistic transport, which contributes to rapid switching and high performance.

2) Compatibility with High-k Dielectrics: Ensures efficient electrostatic control.

3) High Carrier Velocity: Enables abrupt switching.

4) Good Thermal Conductivity: Enhances heat dissipation.

GNRFET Circuit Architecture

This section provides a comprehensive overview of various GNRFET structures and their performance characteristics. Key methods include Doped Channel GNRFET, which improves performance through selective p-type and n-type doping; Schottky Barrier GNRFET (SB-GNRFET), which utilizes metallic Schottky contacts for efficient charge transport; and Metal Oxide Semiconductor GNRFET (MOS-GNRFET), which offers enhanced transconductance but with increased fabrication complexity. Lightly Doped Drain and Source GNRFET (LDDS GNRFET) minimizes leakage currents, while Single Gate (SG-GNRFET) and Double Gate (DG-GNRFET) structures vary in control and performance. Asymmetric Gate (AG-GNRFET) and Electrically-Activated Source Extension (ESE-GNRFET) designs improve performance and reduce tunneling effects. Dual Material Gate (DMG-GNRFET) and Two Different Gate Insulators (TDI-GNRFET) optimize gate functionality to enhance current ratios and reduce leakage. Lastly, Extra Peak Electric Field GNRFET (EPF-GNRFET) modulates channel control and emission by employing dual gates. Table 1 shows the various GNRFET structures, their functions, and performance characteristics

Table 1 Comparative Analysis of GNRFET Structures: Structure, Function, And Performance

GNRFET Structure	Structure	Function	Performance
Doped Channel GNRFET(Sharma, V. K. , 2022).	P-type or n-type doped channel	Enhances carrier propagation; n-type doping improves current	Higher on-current (Ion), stable off-current (Ioff), better switching with n-type doping
Schottky Barrier GNRFET (SB-GNRFET) (Choudhary, S., & Singh, V. 2016)	Metal contacts with Schottky barriers	Charge transport governed by Tunnelling effect	Higher scalability, lower power consumption, lower delay, lower Ion/Ioff ratio with LER
Metal Oxide Semiconductor GNRFET (MOS-GNRFET) (Sharma, V. K. , 2022)	Heavily doped source and drain regions	Functions like a MOSFET; avoids ambipolarity	Better on/off ratio, larger transconductance, higher switching speed
Lightly Doped Drain and Source GNRFET (LDDS-GNRFET) (Choudhary, S., & Singh, V. 2016)	Lightly doped drain and source regions	Reduces 627unnelling and leakage currents	Improved subthreshold swing (SS), reduced ambipolar conduction

Single Gate GNRFET (SG-GNRFET) (Sarvari, H,2012)	Single gate controlling the channel	Simpler control, exhibits short channel effects	Higher cut-off frequency, lower transconductance, poorer saturation
Double Gate GNRFET (DG-GNRFET) (Gholipour, M,2014)	Two gates surrounding the channel	Better channel control, reduces short channel effects	Lower subthreshold swing (SS), higher transconductance, suitable for high-frequency applications
Asymmetric Gate GNRFET (AG-GNRFET) (Naderi, A., & Keshavarzi, P. ,2014)	Gate covering part of the channel	Reduces parasitic tunneling currents	Better SS, improved Ion/Ioff ratio with voltage adjustments
Electrically Activated Source Extension GNRFET (ESE-(GNRFET) Naderi, A. ,2015)	Main gate plus side gate forming a source extension	Reduces Drain-Induced Barrier Lowering (DIBL), controls subthreshold swing	Lower SS, reduced leakage, higher Ion/Ioff ratio
Dual Material Gate GNRFET (DMG-GNRFET) (Naderi, A., & Keshavarzi, P. ,2014)	Gate split into two materials with different work functions	Creates potential barrier, reduces leakage currents	Higher saturation current, better leakage control, increased device lifetime
Two Different Gate Insulators GNRFET (TDI-GNRFET) (Naderi, A. ,2015).	Gate with two insulators of different dielectric constants	Reduces parasitic capacitance, improves gate control	Higher Ion/Ioff ratio, lower leakage current, increased transconductance
Extra Peak Electric Field GNRFET (EPF-GNRFET) (Akbari Eshkalak, M., & Anvarifard, M. K. , 2017)	Two gates with fixed voltage creating an inversion channel	Modulates surface potential, improves channel control	Better control over thermionic emission, reduced tunneling

2. FINFET Circuit

The FinFET (Fin Field-Effect Transistor) technology has undergone significant evolution to address challenges in scaling and performance. This table provides a comprehensive overview of various FinFET structures developed to optimize performance and mitigate issues such as short-channel effects (SCEs), drain-induced barrier lowering (DIBL), and leakage currents. Each FinFET variant is characterized by unique device structures, channel materials, and advancements aimed at enhancing electrostatic control and reducing power consumption. Motorola, IBM, and AMD widely utilize FinFET technology, which operates similarly to traditional MOSFETs. Like MOSFETs, FinFETs are three-terminal devices, comprising a source, drain, and gate terminal, which control the flow of current. The key difference lies in the channel design. Unlike the planar channel in MOSFETs, FinFETs feature a 3D channel structure, where the channel is designed as vertical bars on top of the substrate. This 3D channel structure, known as FinFET, enhances drain current and effectively reduces the channel width to half of the effective channel width. Figure 2 illustrates the 3D structure of FinFETs.

Device Structure: The configuration of the FinFET, which may include vertical MOSFET structures, double-gate designs, or gate-all-around (GAA) architectures. The structure influences how effectively the transistor can control the channel and manage short-channel

effects.

Channel Type: The material used for the channel, such as silicon (Si), silicon-germanium (SiGe), or gallium arsenide (GaAs). The choice of channel material impacts the device's electrical properties, including drive current and leakage characteristics.

Key Characteristics: Highlights of each FinFET type, focusing on aspects such as performance improvements, mitigation of SCEs, and advancements in modeling and fabrication techniques.

Figure 2 FinFET Structure

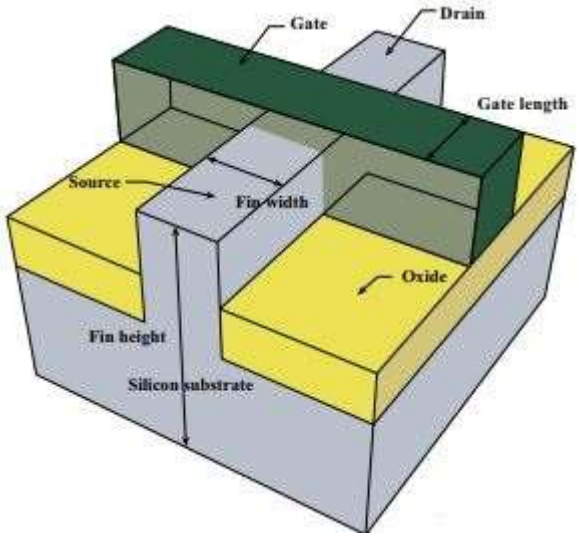


Table.2 below summarizes the key FinFET types, including their structures, channels, and notable features, providing insight into the progress and innovations in FinFET technology.

Table 2 FINFET Device Structures and Channel Types

FinFET Type	Device Structure	Channel Type	Key Characteristics
Fully Depleted Lean-channel Transistor (DELTA)(Chen, Y., ,2013)	Vertical MOSFET with lean channel	Silicon (Si)	Designed to minimize SCEs by ensuring effective device length is larger than the depletion width.
Double Gate SOI MOSFET (Hisamoto, D.,1989)	SOI (Silicon-On-Insulator) with double gate configuration	Silicon (Si)	Uses thin-film technology to address SCEs with device thickness smaller than the depletion layer.
Folded Channel Transistor (Akbari Eshkalak,2015)	Folded channel in a DG SOI MOSFET	Silicon (Si)	Variant of DG SOI MOSFET; reduces SCEs with a gate length of 45nm.
Double Gate (DG) MOSFET (Kaundal, S., & Rana, A. K. ,2019)	Dual gate structure	Silicon (Si)	Improved performance with gate length reduced to 18nm for minimized short-channel effects.

Fully Depleted (FD) SOI FinFET (Huang, X., ,1999)	SOI substrate with fully depleted FinFET structure	Silicon (Si)	Channel surrounded by gates on three sides for enhanced electrostatic control.
Quasi-Planar FinFET (Lindert, N.,,2012)	Planar structure with optimized Fin width	Silicon (Si)	Optimizes DIBL effects with an optimal Fin width to gate length ratio.
Spacer Lithography-Based FinFET(Yeo, Y.-C,2005)	SOI substrate with SiGe heterostructure and spacer lithography	Silicon-Germanium (SiGe)	Uses spacer lithography for uniform Fin width and improved current performance.
Triple Gate FinFET (Talmat, R.,2012)	Triple-gate structure	Silicon (Si)	Reduces gate tunneling current and improves performance compared to quasi-planar devices.
Symmetric High-k Spacer Hybrid FinFET (Pradhan, K. P,2016)	SOI technology with high-k dielectric and UTB	Silicon (Si)	Incorporates high-k dielectric and ultra-thin body for superior drain current and reduced short-channel effects.
Junction-Less Accumulation Mode (JAM) Bulk FinFET(Biswas, K.,,2017)	Bulk FinFET with junction-less design	Silicon (Si)	Optimizes spacer materials and length for improved analog and RF performance.
High K/Metal Gate (HKMG) FinFET (Chew, K. W. J, 2015).	High-k dielectric and metal gate	Silicon (Si)	Examines electrostatic behavior and gate capacitance variations with narrow Fin width.
GaAs-Based SOI FinFET (Baishya, S.,2018)	SOI substrate with Gallium Arsenide channel	Gallium Arsenide (GaAs)	Improves drain current and reduces leakage due to higher mobility properties.
Wavy Design FinFET (Chakkikavil, A.,2017)	SOI substrate with wavy Fin design	Silicon (Si)	Features an ultra-thin wavy design to enhance current driving capability and reduce leakage.
3D Tapered FinFET(Boukortt, N.,,2022)	3D tapered structure with varying Fin thickness	Silicon (Si)	Uses 3D tapering to improve ON current and response time while managing leakage.
GAA FET vs. Bulk Si-FinFET(Vashishtha, V.,,2021)	Gate-All-Around (GAA) vs. Bulk Si-FinFET	Silicon (Si) / Various	GAA FET provides better control and reduced leakage with gate coverage around the entire channel.
JAM-GS-GAA FinFET (Priyanka, Singh, S. K., & Dua, P., 2021).	Gate-All-Around (GAA) with Junction-Less Accumulation Mode	Silicon (Si)	Optimizes aspect ratio and enhances RF/analog performance.
Lightly Doped DMG FinFET Model (Priyanka, Singh, S. K., & Dua, P. 2021)	Double Material Gate (DMG) with lightly doped channel	Silicon (Si)	3D analytical model for electrostatic potential, optimizing DIBL and hot carrier effects.

3. Implementation of Full Adder Circuit Using FINFET, and GNRFET

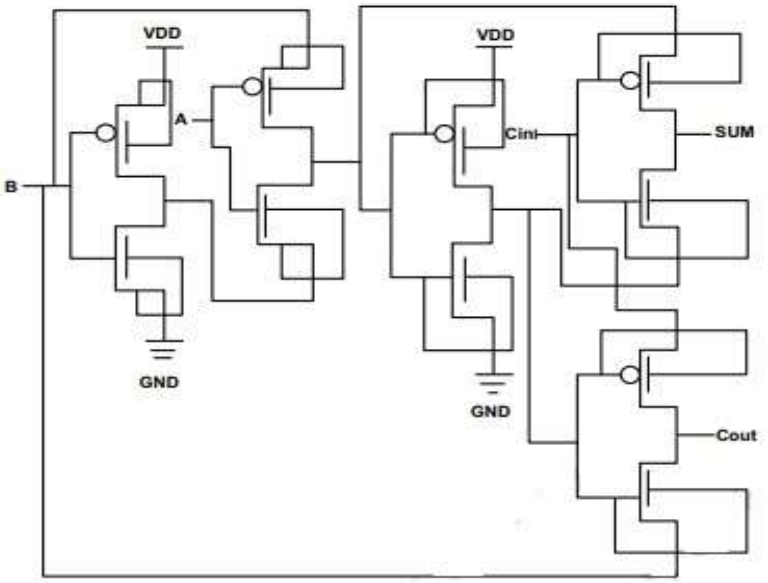
Addition is a fundamental computational operation and is extensively utilized in digital electronics and arithmetic logic units (ALUs) to add numeric values. Typically, a one-bit adder cell is implemented as a full adder, which has three inputs: A,B and C_in. When these inputs are combined, they produce two outputs: Sum and C_out. The relationships governing the Sum and C_out outputs in a one-bit full adder are as follows:

$$\text{Sum} = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = AB + C_{in}\,(A \oplus B) \quad (2)$$

Fig.3. illustrates a 10-transistor (10T) full adder implemented using FinFET technology. This technique aims to reduce power dissipation and delay. The gate is short-circuited in this design. The FinFET adder is realized using 15nm technology. A multiplexer is employed as a selective input and functions as an inverter to execute the carry operation. However, due to threshold voltage loss, the design does not achieve full swing.

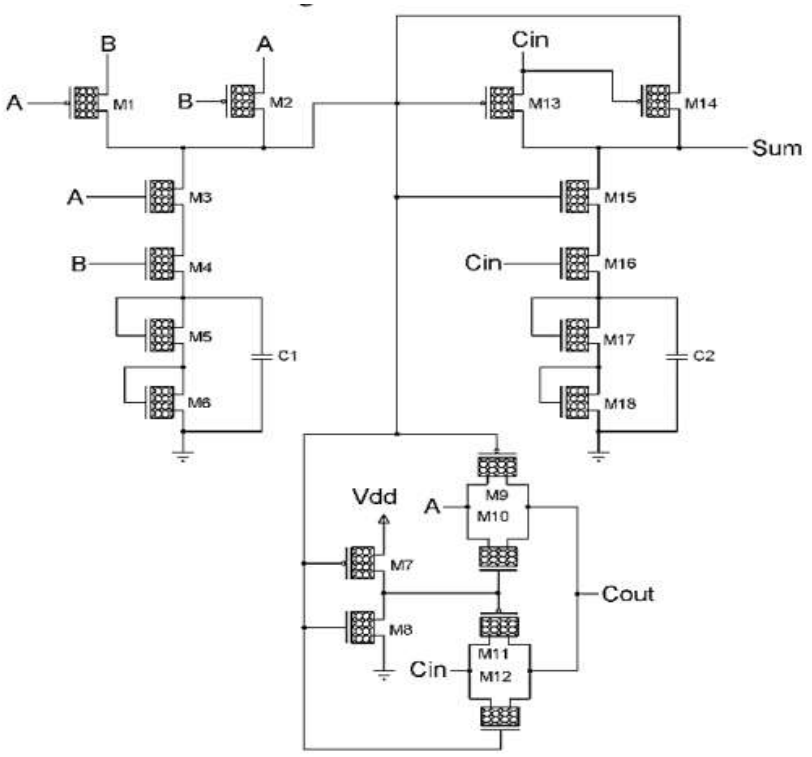
Figure 3 Schematic of the proposed full adder based on FinFET technology



The aforementioned relations can be implemented using two XOR gates and a 2-to-1 multiplexer. Previous designs of full adders utilize two stages of XNOR or XOR gates to generate the Sum logic and a 2-to-1 multiplexer, as discussed in sources. The performance of the full adder circuit heavily depends on the speed and power consumption of the two XOR gates used. By improving the performance of these XOR gates, the overall efficiency of the full adder can be enhanced. An optimized XOR gate based on GNRFET technology is implemented and evaluates its performance within the full adder. Fig.4 presents a schematic of the GNRFET-based full adder, where the proposed XOR circuit uses six GNRFETs and a capacitor. In this design, transistors M1 to M6 form the first XOR circuit, and transistors M13 to M18 form the second XOR circuit, implementing the XOR function without complementary

inputs. This design achieves the shortest possible critical path, significantly reducing delay and power consumption (Priyanka, & Nizamudin, M. 2011; Uma, R., & Sharmila, R. 2011; Priyanka, & Garg, A., 2017). The proposed XOR gate incorporates transistors M5 and M6 (and similarly, M17 and M18) to minimize power consumption, leveraging the technique described in (Chen, Y.,2023). This technique uses two transistors in series and parallel with a capacitor in the downstream network to limit leakage current, effectively reducing power consumption in the full adder circuit(Priyanka, & Nizamudin, M. 2011, Priyanka, Gehlot, S., & Kumar, S. ,2011).

Figure 4 Schematic of the Proposed Full Adder based on GNRFET Technology



3. Results and Discussion

In this study, a GNRFET-based full adder was extensively evaluated and its performance compared to a FinFET-based design. The GNRFET design was simulated using the Synopsys HSPICE simulation tool. Table.3 shows the PDP of FinFET and GNRFET of various supply voltage.

Table 3 Power Delay Product (PDP) Comparison of FinFET and GNRFET at Various Supply Voltages

	FinFET	GNRFET
Supply voltage	PDP	PDP
0.5	35.16	2.3656
0.65	54.031	1.44.3

0.8	1011.1	0.949

Power Efficiency

The results demonstrate a significant power efficiency advantage for GNRFETs over FinFETs. At a supply voltage of 0.5V, the PDP for the GNRFET-based design is 2.3656 fJ, which is approximately 15 times lower than that of the FinFET-based design (35.16 fJ). This trend of lower PDP values for GNRFETs is consistent across all evaluated supply voltages.

Impact of Supply Voltage

As the supply voltage increases, the disparity in PDP between the two technologies becomes even more pronounced. At 0.65V, the GNRFET's PDP is 1.443 fJ, compared to 54.031 fJ for the FinFET, showing an almost 37-fold improvement in power efficiency. When the supply voltage reaches 0.8V, the PDP for the GNRFET further drops to 0.949 fJ, while the FinFET's PDP dramatically increases to 1011.1 fJ, reflecting a more than 1000-fold improvement in power efficiency for the GNRFET.

Scalability and Performance

The ability of GNRFETs to maintain low PDP even at higher supply voltages highlights their potential for use in low-power, high-performance applications. This performance is particularly relevant for emerging technologies that demand both high efficiency and scalability. The ballistic transmission assumption used in the GNRFET model supports these results, indicating that GNRFETs can achieve superior performance in short-channel devices compared to traditional FinFETs.

The comparison between FinFET and GNRFET in terms of PDP across various supply voltages reveals that GNRFETs offer a remarkable improvement in power efficiency. This efficiency, combined with their scalability and performance advantages, positions GNRFETs as a promising candidate for future nano-electronic devices, particularly in applications where energy efficiency is critical.

4. Conclusion

This paper shows that GNRFETs have significant advantages over FinFETs, especially in power efficiency. GNRFETs consistently exhibit a much lower Power Delay Product (PDP) across various supply voltages, thanks to their high carrier mobility and efficient ballistic transport. This makes GNRFETs highly scalable and ideal for future low-power, high-performance applications, particularly in technology nodes smaller than 10 nm. In contrast, FinFETs, while still effective for current technologies, face challenges with higher PDP values as supply voltages increase, which impacts their energy efficiency. As we push the boundaries of semiconductor technology, GNRFETs offer a promising alternative, potentially transforming future nanoscale transistors. Continued research and development will be crucial to fully realize their potential in advanced electronic devices.

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