Nanotechnology Perceptions
ISSN 1660-6795
www.nano-ntp.com

Advanced Architectural Innovations In Double-Gate Mosfets For Enhanced Performance In Vlsi Applications

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Cylindrical Surrounding Double-Gate Metal Oxide Semiconductor Field Effect Transistors (CSDG MOSFETs) are crucial in minimizing thermal effects since they carry a cylindrical configuration that lowers heat generation and provides adequate stability. Therefore, this present study is carried out on the thermal impacts upon CSDG MOSFETs for nanotechnology applications and VLSI circuits. The research analyzes different aspects of CSDG MOSFETs: Thermal resistance, carrier mobility transconductance and overall thermal stability. The results showed the detection of the inner cylinder as well as outer radial section of resistors inside the CSDG MOSFET heat dissipation system's surface coiling turns at 25°C and carry out their tests at this temperature level with operational DC current flow parameters not more than RMS Actual Value. The paper applies a thermal resistance model to evaluate power distribution and discusses the occurrence of thermal noise especially in nanoscale design as well as two-channel designs. For thermal noise analysis, the study uses a Charge-based PSD method that accommodates factors such as channel length and carrier mobility. The research also scrutinises temperature effects on critical parameters like Thermal Resistance (TR), Drain Current (Im), Transconductance (TC) and carrier mobility. It shows that these parameters are very sensitive to temperature changes because while the higher temperatures improve drift current, decrease electron mobility due to high collision frequency. Improvement strategies such as a control circuit in the MOSFET and encompassing cylindrical design have been introduced for better thermal management. The study concludes that CSDG MOSFET designs are more effective at handling thermal impacts than conventional ones making them desirable for high-performing electronic appliances, especially in areas with oscillating temperatures. This comprehensive account outlines the potential of CSDGM; devices to improve the integrity and performance based on VLSI and nanotechnology, thus opening opportunities for bettering future.

Keywords: CSDG MOSFET, Thermal Resistance, Drain Current Analysis, Trans conductance Variation, Temperature Sensitivity, Thermal Stability, Numerical Simulation, Carrier Mobility.

Introduction

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It is fabricated using MOSFET due to its relatively easy design, energy-efficient capabilities, and the simplified manufacturing process of VLSI Circuits. Such features are necessary for portable electronics development [1] and [2]. In contrast, MOSFETs are prone to temperature fluctuations, which may affect their functionality. Tremendously high temperatures affect the molecular motion of carriers within the MOSFET so that speed and functionality fall. Poor temperature management can lead to thermal runaway, a self-reinforcing process between increased temperature and leakage current, causing instability in the MOSFET [3].

High temperatures in MOSFETs, especially when combined with a high voltage supply, as is the case in this study, can result in low values of both drain saturation current and switching speed rates [4]. On the other hand, lower temperatures increase device transconductance and reduce series resistance, which results in better dynamics. These lower temperatures also reduce sub-threshold current and slope, saving power consumption [5]. Nevertheless, the disadvantages of lower temperatures, such as reduced efficiency and reliability, usually prevail over these advantages, which make thermal effects a critical issue [6].

[7] and [8] have assessed the thermal conductivity of MOSFETs with a 65 nm channel length BOX SiO2 in their study. The researchers compared high-k dielectric materials, including diamond and Al_2O_3, to the conventional SiO_2. Furthermore, they examined low-k materials such as air. This study found that substituting BOX with materials such as diamond, which has a thermal conductivity of 800 Wm-1K-1, or using AlN and Al_2O_3 with lower thermal conductivities improves thermal sensitivity and worsens short-channel effects.

[8] and [9] also helped to understand and solve the thermal problems of MOSFET. To achieve better control over the channels, multi-gate transistors were introduced to mitigate thermal effects and reduce leakage current [10] and [11]. Despite these developments, thermal effects still need to be solved. Figure 1 led to a new architecture, namely CSDG MOSFET [12] and [13]. This design significantly decreases the role of the corner effect on “carrier mobility” [14] and reduces contact between the device and the IC board; thus, the generated heat is minimised.

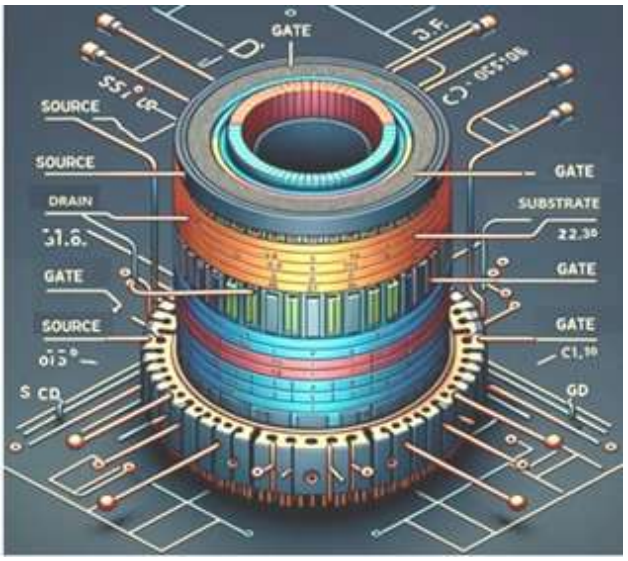

Fig 1: Internal view of 3D CSDG MOSFET [1]

Thermal Resistances in CSDG MOSFET

In our study of the thermal resistances in "Cylindrical Surrounding Double-Gate (CSDG) MOSFET", we have considered earlier models that discuss heat management and their limitations cited in [15] and [16]. The low gate TR ($R_€$) of the CSDG MOSFET impacts the power distribution across the interior and exterior cylindrical shapes. The thermal resistance model covers the channel source and drain total resistance but pays little attention to the MOSFET body. The thermal resistance within the inside cylindrical section ($R_¢$) and the external cylindrical section ($R_{¢ext}$) can be expressed as follows:

For the internal part: $R¢ = R¢S + R¢CH + R¢D$ (1)

For the external part: $R¢ext = R¢CH(2) + R¢S(2) + R¢D(2)$ (2)

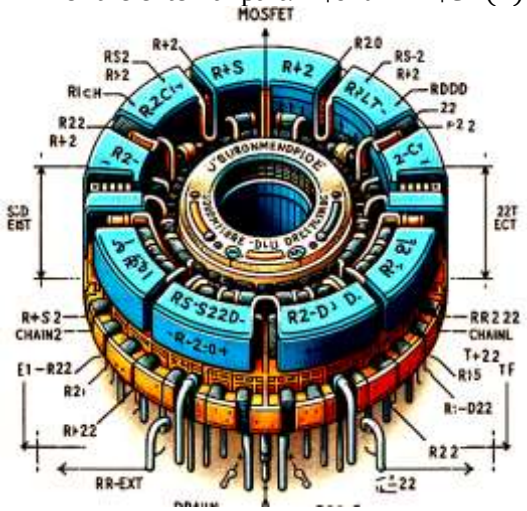

Fig. 2: Internal Cylindrical Part [2]

Fig. 2 includes the internal cylindrical section (labeled R¢) and the external cylindrical section (labeled R¢ext), along with their respective components such as source, channel, and drain. The total thermal resistance R€ is also denoted.

The following symbols denote the respective resistances of sources $R_{¢}$ and $R_{¢ext}$, channel $R_{¢CH}$ and $R_{¢CH(2)}$, and drains for both exterior and interior components as $R_{¢D}$ and $R_{¢D(2)}$.

Considering the parallel arrangement of its interior and exterior, the total TR, referred to as "CSDG MOSFET", is found.

$$R_{€}=\frac{[(R¢S+R¢CH+R¢D)(R¢S(2)+R¢CH(2)+R¢D(2))]}{[(R¢S+R¢CH+R¢D)+(R¢S(2)+R¢CH(2)+R¢D(2))]} \quad (3)$$

$R_{€}$ represents a total thermal resistance

By this study, the paralleling of these "CSDG MOSFETs" effectively reduces thermal resistance; thus, this value is lower than other previously investigated "MOSFETs". The lower TR in the CSDG MOSFET is beneficial mainly when used in nanotechnology.

Thermal Noise (TN) in CSDG MOSFET

Decrease in dimension of MOSFETs, increases TN, this in turn affects their operating efficiency. Specifically, the CSDG MOSFET features dual-channel architecture and functions at the nanoscale [17] and [18]. Contrary to popular belief, the thermal noise in short-channel MOSFETs does not exceed too much compared to more extended channels [19] and [20]. In CSDG MOSFETs, the thermal noise remains significant even with zero gate voltages as they have nanoscale dimensions and dual-channel configuration.

A new methodology is presented to reduce the TNin CSDG MOSFETs. This approach uses the charged-based "Power Spectrum Density (PSD)" technique to assess theTN of MOSFETs. As references [21] and [22] state, the thermal noise is affected by charge carrier mobility, temperature, total charge along the channel, and channel length. This model intended for long-channel MOSFET is well applicable to short-channel CSDG MOSFETs because of their high transconductance values. It is expressed as:

$$\epsilon= \frac{4\alpha\tau\Theta q}{W\hat{}2} \quad (4)$$

τ denote the charge carrier mobility

Θ the temperature

W represents length of the channel.

In this model, the charge flow across channels is mostly unaffected by the "drift current (v_r)." However, the prevalence of "diffusive random current (DRC)" in charge transport has a direct influence on the increase of thermal noise in this device. This is particularly true in the case of CSDG MOSFET's linear (ohmic) region.

A critical element in the progressive channel region of CSDG MOSFETs is carrier mobility loss due to lateral electric fields, which greatly influence thermal noise in these devices [31]. The thermal noise might be represented or simulated as:

$$\epsilon_n^2 = 4pq^2G\Delta\phi\frac{H}{W} \quad (5)$$

p-carrier density
G-Diffusion constant.
$\Delta\phi$ - Band width
H– Channel width
I_m is influenced by reduced carrier mobility (CM), is computed as:

$$I_{m=} \tau pHq(V)\frac{\partial V}{\partial W}\Bigg/\left(1+\frac{\frac{\partial V}{\partial W}}{F\_B}\right) \quad (6)$$

By performing the process of integration about the applied voltage along the channels, the noise levels are transformed:

$$\Delta I_m = \epsilon_n \frac{\tau pHq(V)\Delta V}{W+\frac{Vds}{F\_B}} \quad (7)$$

This equation accounts for the amount of charges, channel charge, mobility and width of the gate voltages applied for CSDG MOSFET. Thus, the total noise for two "CSDG MOSFET's" channels is presented below.

$$e_n^2 = \sum [\Delta I_m]^2 \quad (8)$$

$$e_n = \sum 4pq2G\Delta\phi\frac{H}{W}.\frac{gth\ \Delta V2}{W+\frac{Vds}{F\_B}} \quad (9)$$

This study focuses on the increased Thermal noise current in CSDG MOSFETs caused by carrier heating effects at high applied voltages and in the gradual channel approximation. This is relevant to using these devices in nanotechnology applications, where thermal noise plays a crucial role in performance.

Thermal Impact on the CSDG MOSFET Parameters

The efficiency and performance of MOSFETs are highly influenced by temperature changes [23]. Self-heating in these devices can change their operating environment and, consequently, their effectiveness and reliability. However, an improved CSDG MOSFET design has been developed with these constraints: a cylindrical structure to reduce board contact and heat generation.

This analytical study focuses on the CSDG MOSFET regarding critical parameters such as Im, electron mobility (Em), and T_c. The research looks at how temperature changes impact these parameters. The estimation of the CSDG MOSFET device's overall performance is contingent upon the temperature-dependent parameters, which is computed using mathematical modelling.

Thermal Effect on Drain Current

The rise in temperature affects the movement of electrons, which also impacts the drain current for MOSFETs. The only crucial scattering mechanism in the context of undoped CSDG MOSFET channels is electron-electron collisions.

An increase in temperature boosts the drift current. Applying voltage across the CSDG MOSFET gates generates an electric field along the channels, exciting the electrons. However, when the temperature increases, an initial rise in the speed of electrically charged particles is observed. There is a gradual decrease in electron mobility over time due to the higher collision frequency inside cylindrical channels. This slows down the speed at which electrons move from the source to the drain. The relationship between the drift velocity (v_r) and the carrier mobility CM is directly established by references [22] and [23]

$$v_r = \tau \cdot F \quad (10)$$

$$I_r = \frac{pq\tau 2\pi(c+d)V}{W} \quad (11)$$

V-Voltage applied.
W- Channel length

$$I_{diff = E' q}\, \pi(c + d)\text{^}2 \left[-\frac{dp}{dW}\right] \quad (12)$$

I_{diff} represents the diffusion current,
E' is the "diffusion constant"

$$E' = \tau\Psi \quad (13)$$

Ψ -Thermal voltage.

$$\Psi = \frac{h\Theta}{q} \quad (14)$$

.

h - Boltzmann's constant
Θ- temperature

Thermal Effect on Transconductance

Figure 3 analyze the CSDG MOSFET's transconductance is crucial, especially when assessing how sensitive it is to temperature. Transconductance measures the relationship between the current transfer from the drain and the voltage across the gate and source. This value can be obtained by utilising "the derivative of the Im" with refer to "the gate-source voltage", When the V_{ds} is constant. Equations (5) & (6) illustrate this method.

The transconductance, confirmed through simulation, illustrates a notable increase with a decrease in temperature, aligning with the behaviour observed in saturation current. Transconductance remains relatively stable with temperature variations up to approximately 100 K. Beyond this point, a gradual decrease is observed, becoming more pronounced past 150 K. This pattern suggests that while the CSDG MOSFET demonstrates efficiency at

temperatures below 100 K, its reliability diminishes at temperatures exceeding 150 K. Future sections will explore measures to mitigate this issue.

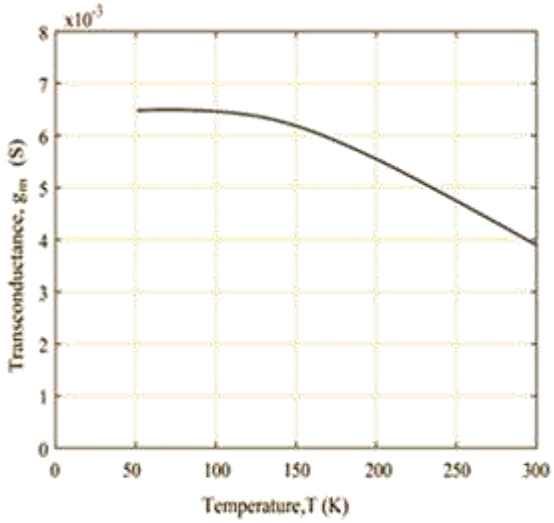

Fig. 3: Thermal Effect on Transconductance

Thermal Effect on Carrier Mobility (CM)

Temperature primarily affects the conducting channels' Em in the CSDG MOSFET. The Em is indicator of gadget's efficiency. CM is influenced by elements such as "Electric Field Strength", different scattering mechanisms, and temperature. The low "threshold voltage" is the distinguishing characteristic of the CSDG MOSFET, which leads to an increase in Em until it reaches a saturation point, at which time Im stabilises.

The ideal length of the conducting channels and the undoped state are two essential components of this complex MOSFET design. The absence of impurity doping minimizes several scattering mechanisms, even though electron-electron collision is still the primary factor. Temperature is an essential indicator of mobility. The correlation between increasing temperature and rising drift current and carrier mobility has been proven at cryogenic temperatures.

$$F= \frac{\lambda(c+d)}{2\pi cd\sigma} \quad (15)$$

F– Electric Field
λ – electron per unit
c , d – internal and external radii
σ - permitivitty
v_r- drift velocity

$$\tau= \frac{2\pi\sigma}{\lambda}\left[\frac{cd}{c+d}\right] \quad V_{rCSDG} \quad (16)$$

$$\tau = \frac{2\pi\sigma}{\lambda\Theta}\left[\frac{cd}{c+d}\right] \quad V_{rCSDG} \tag{17}$$

The temperature and CM in the CSDG MOSFET exhibit an inverse correlation. Therefore, an increase in mobility is seen as temperature decreases. However, when temperature rises, increased mobility leads to more frequent electron collisions, thus reducing mobility and affecting other device parameters. Although the CSDG MOSFET is temperature tolerant, temperature should not be higher than 100°C to ensure device reliability and avoid damage.

THERMAL STABILITY IN CSDG MOSFET

One of the most important problems in electronic devices, especially MOSFETs, is thermal instability. Such instabilities may lead to poor performance outside the SOA due to variability in thermal variables arising from internal and external sources. Internal heating occurs due to the strong adhesion of passive elements in a microchip. Simultaneously, the external heats are generated from variations in environmental temperature and physical contact between MOSFET and its surroundings [22] and [23].

Many innovative ideas have been formulated for handling such thermal complications in MOSFETs. Another solution is integrating a control element in the MOSFET to regulate and respond to temperature variations. On the other hand, this may lower the integrity of such a device. The architecture of the CSDG MOSFET handles unprecedented thermal problems. It contains an empty internal system, which increases the airflow and decreases heat accumulation in the interior part. This modification results in better thermal stability than the previous models.

The CSDG MOSFET's round design also minimizes contact with the mounting board. The heat sink makes it possible to reduce the thermal transfer process of the board. The power dissipation and the circuit's performance in the absence of a heat sink:

$$M = R_{€} I^2 \tag{18}$$

M - Power dissipated

$$M_{max} = \frac{\Theta max - \Theta amb}{R€} \tag{19}$$

M_{max} -Maximum amount of power dissipated.

R€- TR of the CSDG MOSFET

Θ_{max} - the maximum operational temperature, and

Θ_{amb} - the ambient temperature.

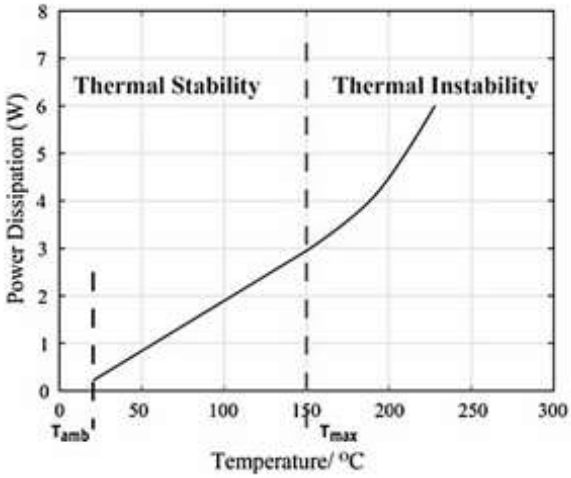

Fig. 4: TR of CSDG MOSFET

In essence, this study offers a comprehensive analysis of the thermal effects on CSDG MOSFETs. It highlights the importance of thermal resistance modeling and its impact on device parameters under varying temperatures shown in figure 4. While the CSDG MOSFET exhibits improved thermal stability, accommodating both internal and external heat generation, challenges remain in analyzing the thermal noise and its impact on device performance. Future research will focus on enhancing the CSDG MOSFET's thermal stability and developing more robust models for thermal noise in the context of nanotechnology and VLSI applications.

Algorithm

1. **Initialize Constants and Parameters**
   Set the Boltzmann constant **H**.
   Set the charge of an electron **q**.
   Define the MOSFET parameters like carrier mobility **CM**, gate-source voltage $\mathbf{V_{GS}}$, drain-source voltage $\mathbf{V_{DS}}$, channel length $\mathbf{W^2}$**,** channel width **Z**, oxide capacitance per unit area **Cox**, and threshold voltage **Vth**.
2. **Define the Temperature Range**
   Create a range of temperatures (e.g., from 0K to 300K) over which the analysis will be conducted.
3. **Prepare for Data Collection**
   Initialize arrays or lists to store the calculated values of drain current (**Id_arr**) and transconductance ($\mathbf{g_{m\_arr}}$).
4. **Temperature-Dependent Analysis**
   For each temperature **T** in the defined temperature range:
   Calculate "Threshold Voltage ($\mathbf{V_{th\_T}}$)" Shift: Adjust the $\mathbf{V_{th\_T}}$ based on the current temperature **T**.

Calculate Drain Current (I_D): Use the MOSFET parameters and the temperature-adjusted threshold voltage to calculate the drain current at the current temperature.
Calculate Transconductance (g_m): Compute the transconductance using the MOSFET parameters, temperature-adjusted threshold voltage, and current temperature.
Store Calculated Values: Append the calculated values of I_D and g_m to their respective arrays or lists.

5. **Plotting the Results**

Drain Current vs. Temperature Plot: a. Plot the temperatures against the calculated drain current values. b. Label the axes (Temperature and Drain Current) and provide a title for the plot.
Transconductance vs. Temperature Plot: a. Plot the temperatures against the calculated transconductance values. b. Label the axes (Temperature and Transconductance) and provide a title for the plot.
Display the plots for analysis.

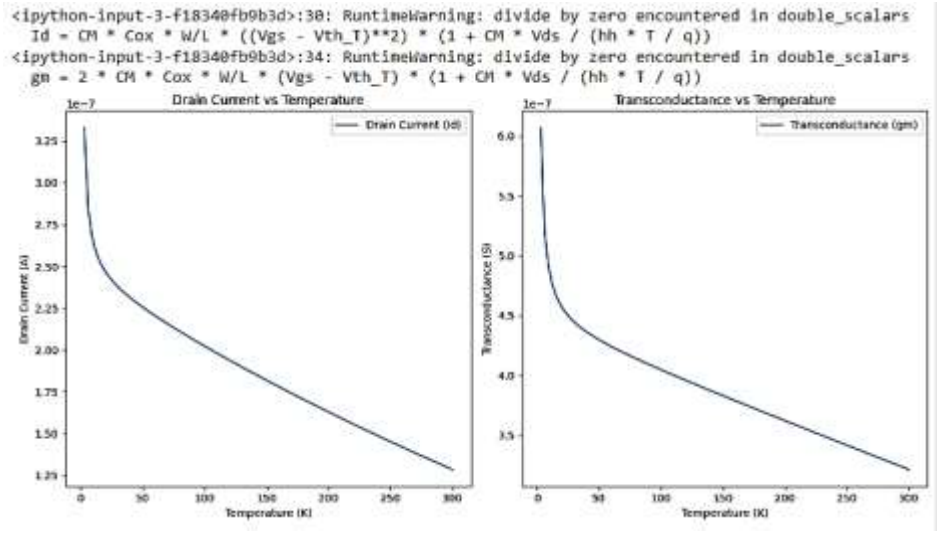

Fig. 5 (a) : Drain Current vs. Temperature Plot, Fig. 5 (b) : Transconductance vs. Temperature Plot

Drain Current vs. Temperature Plot

Figure 5 (a) plot shows how the drain current (I_D) varies as the temperature changes. A rise in temperature typically results in a simultaneous rise in the I_m. This is due to the enhanced CM at higher temperatures, which facilitates the movement of charge carriers (electrons or holes) across the MOSFET's channel. However, there's a limit to this behavior. Beyond a certain temperature, the performance might degrade due to increased carrier scattering and other thermal effects.

Transconductance vs. Temperature Plot

Figure 5 (b) plot illustrates the change in transconductance (g_m) with temperature. Transconductance is a measure of the MOSFET's ability to control the input voltage, which is nothing but gate-source voltage and the output current. A higher transconductance indicates better control. The plot results reveal that transconductance could first increase due to increased carrier mobility with an increased temperature. However, as the temperature increases, transconductance declines, which may mean MOSFET's efficiency in controlling current flow decreases. This may be due to increased carrier scattering and thermal noise at higher temperatures.

Key Points

Thermal Sensitivity: Both plots draw attention to the thermal characteristics of MOSFET. Identifying this sensitivity is essential for designing circuits that work effectively in different temperature ranges.

Optimal Operating Temperature: There is an optimal temperature range where the MOSFET operates most efficiently, managing both increased mobility (corresponding to increased current and transconductance) and too-high temperature, which increases scattering or noise.

Design Considerations: The unique design of such MOSFET should be considered for applications in very low or high temperatures to enable it to operate reliably. This may include the materials, device structure variants, and thermal management techniques.

Conclusion

The detailed analysis of CSDG MOSFET has led to exciting results related to the thermal aspects of technology dealing with MOSFET. The novel CSDG MOSFET architecture has been noted to overcome thermal instability issues, a common phenomenon in conventional designs. Thermal resistance, carrier mobility transconductance, and full-area total thermal stability of the CSDG MOSFET were investigated from different angles.

The analysis observed that CSDG MOSFET performs better in changing temperature conditions, especially where very low temperatures below the cryogenic level are required. A hollow structural core and cylindrical shape are some of the features that help reduce adverse heat effects inside and outside. The modifications enhance the keeping of a steady temperature and provide high reliability in operation for this device.

Additionally, the study gave information on mathematical modeling for specific critical parameters to CSDG MOSFET regarding their behavior under thermal stress. The device redesign alterations and modifications have successfully addressed challenges associated with the heat generated, inside or outside.

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