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Design and Implementation of SRAM Cells using High K-Metal

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Data and instructions that are kept in electronic digital computers refers to the Computer memory, both temporarily and permanently. Significant advances in technology have made it possible to integrate enormous complexity into a single chip. In the design of electronic components, fundamental characteristics including tiny feature sizes, less power consumption, economical, and good performance have become crucial factors. The primary factor behind SRAM's power consumption is leakage current. It is estimated that SRAMs occupy around 60% of the chip area. In response to these changing needs a Static Random Access Memory (SRAM) architecture that lowers leakage current when performing read/write operations using the High-K Metal Technique is presented in this study. High-K Metal logic is incorporated into the design to improve overall performance and reduce leakage current. Due to the scaling of complementary metal oxide semiconductor (CMOS) transistors, gate dielectrics with a high dielectric constant (high-k) must be utilized in place of SiO2. Device reliability is severely hampered by electron tunneling effects and large leakage currents when the SiO2 gate thickness is lowered below 1.4 nm.

Keywords: High-K metal, read and write access delays, threshold voltage, power consumption, delay.

1. Introduction

Circuits which are highly integrated are being developed as a result of technological scaling, especially for portable and Internet of Things (IoT) devices. Over the past few years, low-power operation has become the primary focus of logic circuit design. SRAM is a popular option for cache applications in electronic devices and microprocessors. Its superiority over Dynamic Random Access Memory (DRAM) is apparent. The modern electronic devices, optimized for specific applications such as object tracking, video processing, multimedia, and medical experiences a growth in computing complexity. However, higher power consumption is a consequence of this surge, and this is a crucial factor in the design and optimization of these devices. Managing the limitations of SRAM power usage becomes essential to sustain the delicate balance between computational power efficiency. Strategic actions are taken to address this issue; one strategy is to lower threshold voltage (V_{th})or the

supply voltage (Vdd). SRAM and power considerations have a symbiotic relationship that is prominent in today's world of specialized electronics.

The main goal is creating an SRAM with various logical designs so that performance with respect to speed and power consumption can be compared. The main focus of the study is a comparison of bulk and high-k CMOS. Effectiveness in speed as well as gate leakage current reduction, high-k shows a features which enhances performance by optimizing transistor sizing. The implementation ensures that the access time of low-power SRAMs are compared to that of regular DRAMs. Transistor scaling down are spreading more widely with growing concern of higher power and energy dissipation Static power and dynamic power make up the total power dissipated in a CMOS logic gate. Transistors that are scaled down have lower dynamic energy each cycle,but they additionally have higher leakage current, which causes a large rise in static power dissipation. Energy density constraints compete with digital circuit speed. Although features with smaller sizes can be more integrated and less expensive, energy density must be managed.

"The device performance in the 21st century high-k gate dielectrics and metal electrodes for gates will be required for high-performance and low-power CMOS applications in the 45 nm node and beyond," states Moore's law of scaling. Future logic applications can benefit from high-performance high-κ/metal gate transistors with minimal gate dielectric leakages if metal gates with "correct" task associated functions are employed to supply the proper transistor threshold voltages and mitigate the mobility degradation issue.

The effective demonstration of high-performance logic transistors using high-mobility non-silicon gate material with high I_{ON}/I_{OFF} ratios requires high-κ metal and gate dielectrics as depicted in Figure 1. Gate-oxide scaling has long been seen as an eventual restriction for gate oxides below ~2nm gate dielectric thickness, pertaining toother causes of leakage. It is believed that gate leakage would equal and even exceed transistor off-current leakage when oxides thicken to the level of several atoms, either threshold voltage (Vth) or the voltage (Vdd). SRAM and power considerations have a symbiotic relationship that is prominent in today's world of specialized electronics.

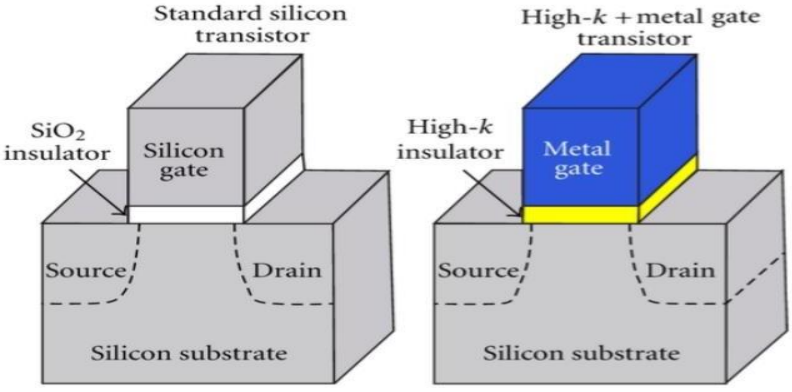

Figure 1 FET Gate stack

Concerns of higher power and energy dissipation resulting from transistor scaling down are becoming more prevalent in this domain. Static power and dynamic power make up the total

power dissipated in a CMOS logic gate. Transistors that are scaled down have lower dynamic energy each cycle, but they additionally have higher leakage current, which causes a large rise in static power dissipation. Energy density constraints presently compete with digital circuit speed. Although reduced feature sizes can lead to benefits such as increased integration and reduced expenses, energy density management becomes crucial.

Low power applications arise as a second driving force in SRAMs, which are designed in order to handle the dual objectives of offering a quick interface with the CPU and replacing power-intensive DRAMs. Under these conditions, SRAMs are often used in portable devices because their low-power standby current significantly exceeds the DRAM refresh current. Because low-power SRAMs are designed to maintain access times that are equivalent to those of regular DRAMs, their usefulness in applications where power efficiency is paramount is reinforced.

2. Related Works

Kavitha, S. et al. [1] discussed the variety of designing techniques for SRAM design for low power applications was covered in detail in the paper that was given. Practical solutions based on both CNFET and CMOS technology are presented in this work. Because of this application, the CMOS technology performs not function as intended in light of the 32 nm channel length. It resulted in undesirable consequences as mobility degradation and short channel effect at 32 nm channel length, among others. The use of CNFET-based SRAM cell design techniques gets around this restriction. Thus, the study demonstrates that, when using CMOS technology, CNFET-based Multi-Threshold SRAM design outperforms conventional SRAM cells. The power reduction approaches will be integrated into the suggested design to further enhance it.

Xue,X.; Sai Kumar et al.[2] in this work, a 6T SRAM cell in CMOS technology was used to develop and analyse a 1 KB SRAM array in bit orientation. It can store 1024 bits in total. With consideration for tiny feature sizes, minimal leakage, and low power consumption, a 1 KB SRAM memory array was recommended. When all factors were taken into account, it was discovered that there was a considerable difference in the power consumption of the 1 KB-SRAM based memory during the read and write operations. A 6T SRAM cell with a minimum leakage current of 18.65 pA and an average latency of 19 ns was used to implement the array structure. The read and write operations utilized as the write driver for low-power applications used 48.22 _W and 385 _W of electricity, respectively. The performance characteristics of the CMOS-based SRAM arrays, including the power dissipation during read and write operations, were compared with those of previous research. This study was validated using the Cadence Virtuoso tool and CMOS 22 nm technology.

Renren Xu et al.[3] discussed a comprehensive study is conducted into the technology of interfacial Al2O3 doping HfO2 laminated stacked layer via controlling ALD cycles. A significant VFB offset value of +360 mV was found at the high interfacial Al2O3 doping. Not decreases from 7.6 × 1011 cm2 to 6 × 1010 cm2, and EWF might vary from 4.97 to 5.206 eV as the degree of interfacial Al2O3 doping increases. Further, there had been significant growth in Dit, TDDB, and PBS, and NSS is being effectively controlled. The results of the experiment demonstrate the viability of our approach and its ability to

enhance the device's interface quality while enhancing the metal gate electrode's EWF, which is one of the key technologies for manipulating p-type HKMG MOSCAPs in future scaling CMOS technology nodes with lower process cost.

Yi-Ju Yao et al.[4] discussed the ferroelectric characteristics of the TiN/Fe-HZO/SL MIS capacitor were verified by measuring the C-V and P-V behaviors at various temperatures and by GIXRD analysis. The devices featuring a Fe-HZO gate insulator had significantly better performance, attaining ION/IOFF > 1.0 × 107, DIBLn = 26.4 mV/V, DIBLp = 37.6 mV/V, and SSmin,n = 62.4 mV/dec. SiGe/Si SL Fe-FET CMOS inverter operation was shown; a maximum gain of 111.4 V/V and a promising VTC were attained. The potential for expanding CMOS technology was proven by a SiGe/Si SL Fe-FET simulated using cutting-edge technology. Thesefindings imply that SiGe/Si SL Fe-FETs have a great deal of potential for usage in high-performance, low-powerapplications.

C. Gastaldi et al.[5] demonstrated a CMOS-compatible double-gate Fe- JLFET operating as a novel energy-efficient tripartite synapse with the unique possibility to highly tune the synaptic weight by the back gate,similar to astrocyte neuromodulation. The ferroelectric functionality of the integrated Si:HfO2 was firstly verified electrically and then electromechanically using PFM. Then synaptic behaviour was experimentally provenwith different synaptic schemes applied on the ferroelectric top gate: amplitude modulation, pulse width modulation, and identical pulses. The control with back-gate linear dielectric is shown to act as an astrocyte functionality, offering additional tunability of the PCS up to 400×. Finally, we validated synaptic plasticity until 2000 cycles in great advance to previous reports with the same technology.

Honggyun Kim1 et al. [6] presented a novel energy-efficient tripartite synapse that is CMOS-compatible and has the unique ability to fine-tune the synaptic weight via the back gate, akin to astrocyte neuromodulation. Using PFM, the integrated Si:HfO2's ferroelectric functioning was first confirmed electrically and then electromechanically. Next, using several synaptic schemes—amplitude modulation, pulse width modulation, and identical pulses—applied to the ferroelectric top gate, synaptic activity was experimentally demonstrated. It is demonstrated that the back-gate linear dielectric control functions as an astrocyte, providing the PCS with additional tunability up to 400×. Ultimately, we verified synaptic plasticity up to 2000 cycles, which is a significant advancement above previous research using the same methodology.

Ning Liu, Jiuren Zhou et al.[7] discussed, the effect of photogenerated-carriers assisted Fe-switching was used to experimentally construct the CMOS compatible 1C-architecture HfO2-based ferroelectric optoelectronic memcapacitors (FOMs), demonstrating highly integrated capabilities of photoelectric perception and storage functions. These devices have a lot of potential to be important enablers for future ultra-low power Internet of Things and edge computing applications because of their outstanding reliability and capacity for in-memory sensing and computing. Erfan Abbasian et al paper [8] describes the creation of a state-of-the-art SRAM cell designed for smartwatches, where power efficiency is a crucial factor. A number of novel features were includedin the suggested design, known as SE10T, such as a read-decoupling method to improve RSNM, a feedback- cutting mechanism to improve WSNM, and a stacked pull-down structure to reduce leakage power. Thesuggested design

obtained a significant increase in ION/IOFF ratio by eliminating RBL leakage and adopting a reading approach with only one transistor. The suggested design demonstrated at least 1.04×, 1.01×, 1.12×, 1.25×, 1.15×, and 1.22× improvement in RSNM, WSNM, TRA, leakage power, dynamic power, and ION/IOFF,according to results at VDD = 0.4 V. It also displays the lowest Vmin = 0.292 V. However, it showed a 1.02× lower HSNM than that of ST10T, offers 1.18×, 1.14×, and 1.13× higher TWA compared to 6T, ST10T, and DW10T, respectively, and consumed 1.56×, 1.07×, and 1.05× higher layout area in comparison with 6T, TGRD9T, and DIRP10T, respectively.

Vijay Kumar Sharma [10] discussed the fundamental concepts of several circuit level leakage reduction strategies are presented in this review study.by taking into account a CMOS NAND3 gate, a comparative analysis of the methodologies is also carried out at the 16 nm technology node.

Battery-operated portable devices are becoming more and more important because of their broad range of applications. strong battery backup and quick speed and compact design are essential performance metrics to evaluate the efficacy of the portable systems. Device scaling improves both the performance and the size of the systems. However, SCEs brought about by device scaling result in significant leakage power. Trade-off therefore happens between the performance metrics. With the use of Cadence's tools and the LP BSIM4 PTM model file for the transistors, logic circuits are constructed and analyzed. For each approach, the important parameters are evaluated, including leakage power dissipation, latency, PDP, and uncertainty. Based on all performance characteristics, the comparison analysis demonstrates that the INDEP technique outperforms the others. The INDEP technique reduces leakage power by 90.53% with a 1.21× delay penalty as compared to the traditional NAND3 gate. PDP and uncertainty values are improved using the INDEP approach.

3. High –K Dielectric in MOSFETS

To significantly reduce the gate leakage current in the CMOS gate dielectric, it is generally accepted that a novelhigh-k dielectric material made of gate oxide has replaced traditional SiO2. The standard gate oxide SiO2 is getting close to its thickness scaling limit because of ongoing reduction of the size of CMOS chip for enhanced speed and reduced power consumption. To lower the gate leakage current and offer high ON current, other dielectric materials with a higher dielectric constant, k, and hence a larger physical thickness than that of SiO2. Mobility of transistor channels in high-k dielectric materials is comparable to that of SiO2, and they have an 1.0 nm EOT with minimal gate oxide leakage and appropriate threshold voltages for transistor, n and p-channel MOSFETs expressed in Eq. (1) . For a device designer, because specific material does not concern, it is convenient to specify a new oxide's electrical thickness expressed in terms of its "equivalent oxide thickness," orequivalent silicon dioxide thickness (EOT).

$$\mathrm{EOT} = \left(\frac{3.9}{\mathrm{K}}\right) \mathrm{Thigh} - \mathrm{k} \tag{1}$$

where 3.9 and k represent SiO2's static dielectric constant , Thigh-κ is the high-κ materials physical thickness . The capacitive coupling amid the gate and the substrate has been grown

over the years by reducing the gate- dielectric thickness less than 2nm. Capacitance of a Dielectric given by Equation (2).

$$C = K\,\varepsilon 0\,A/t \tag{2}$$

where A is the area, t is the oxide thickness, K is the relative dielectric constant, and □0 is the permittivity of free space.

Table 1 summarizes the other high-k dielectric materials, The k value, energy band gap, and offset between the conduction and valence bands. In comparison to reported band gaps ranging from 5.16 to 7.8 eV, SiO2 has a huge band gap of 9 eV, which is sufficiently large for both conduction and valence band offsets. The decrease in threshold voltage with decreasing channel length and increasing drain voltage is frequently used as a metric of the SCEs in the evaluation of CMOS cutting edge technology. This negative threshold voltage roll-off effect is the hardest barrier to overcome in the future design of MOSFETs [18].

Equation 3 represents the function of the various parameters that determine the threshold voltage.

$$V_{TH} = V_{TH0} + K1\left[\sqrt{|2\varphi_S| + V_{BS}}\right] - \sqrt{|2\varphi_S|} - K2V_{BS} + \Delta \tag{3}$$

Where, V_{TH0} is the zero-body bias threshold voltage, K1 and K2 are the first and second order body bias coefficients, $2\phi S$ is the surface potential, the body to source voltage is called V_{BS} and shows the small change within the device's parameters.

The key feature of a high- κ material is its high κ value. A high-κ material has a greater physical thickness compared to SiO2 for the similar EOT (refer equation 4). Because of this large thickness, the tunnelling current issignificantly reduced. Moreover, the material with high-κ can be further scaled down for future generations of technology. The κ value should be over 12, preferably 20-25, to satisfy the scaling requirements.

$$K = n^2 + \sum \frac{Ne^2 Z_2^T}{m^2 w_{TO}^2} \tag{4}$$

However, a high-κ material with κ larger than 25 is ruled out for the following three reasons. First, the κ valuearises from the lattice contribution.

Table 1 Comparing SiO2 with alternate dielectric materials

Dielectric material	Dielectric constant (k)	Energy band Eg(Ev)	Conduction band offsetΔEc(eV)	Offset of the Valence band ΔEc(eV)
SIO_2	3.9	9	3.5	4.4
Si_3N_1	7.5	5.3	2.2	1.8
AI_2O_3	10	6	3	4.7
$LaAIO_3$	15	5.6	1.65	3.25
ZrO_2	25	5.8	1.4	3.3
HfO_2	25	6	1.5	3.4
TiO_2	40	3.5	1.1	1.3

The power constraints resulting from the increased gate leakage caused scaling of the gate oxides to slow downat the 90nm and 65nm nodes. A gate dielectric in combination with a greater dielectric constant (high-k) has been introduced to get around issue at the 45nm technology. This allowed for a 0.7x scaling of the gate oxide layer thickness (Tox) and a >25x reduction in gate leakage. High-k materials aid in reducing gate leakage problems, enabling the creation of transistors that are smaller and require less power. Although introducing new materials necessitates modifications to the manufacturing process, there are performance and power efficiency benefits 90nm metal gate with high-k CMOS technology is applied to construct SRAM cells with various transistor schemes. The gate oxide's scaling halted at the 90nm and 65nm nodes because to power constraints brought on by the rise in This article looks at high-k and bulk technologies at 90 nm. Using various transistor counts, such as 7, 8, 9, 10, and 10 transistors, SRAM cells are engineered for both bulk and High-k CMOS technologies.

Transistor gates are designed using High K metal and high dielectric material, like HfO2 hafnium dioxide, to minimize current leakage, increase size, and maximize power utilization. Better capacitance can be achieved without adding physical thickness in high-k materials since they have a greater dielectric constant than SiO2.In order to preserve the stability of data storage in SRAM cells, High-k technology is employed to employ thicker dielectrics. By utilizing high-k technology, switching speeds in SRAM can also be increased. In silicon technology, the silicon-based material (SiO2) value k, or 3.9, is the standard. Dielectrics with k > 3.9 are called "high"-k dielectrics, whereas those with k < 3.9 are called "low-k" dielectrics. The dielectric, which is often silicon dioxide, is a quite thin layer of insulation that sits between the current-flowing channel and the metal gatetransistor's electrode. There are two physical modifications: in a normal transistor (1), the high K transistor metal gate is used to link the high K dielectric, and a polysilicon gate is utilized to connect with the gate material. (2) A High K layer of dielectric is utilized in place of the SiO2 dielectric. This type of transistor is mostcommonly used for nanoscale transistors and is known as a high K-metal gate transistor. Studies have shown that emploting a higher K dielectric value in place of the SiO2 dielectric can significantly improve the reduction of leakage current. These substances can provide greater capacitance without adding physical thickness because they have a higher dielectric constant (k) than SiO2. Traditional polysilicon gates are replaced using metal gates,which are often comprised of metals like copper or tungsten. Better conductivity and transistor control are offered by metal gates. Tox scaling in conjunction with the ideal work function metal gates results in outstanding.The NMOS and PMOS short channel effects (SCE) and drain induced barrier-lowering (DIBL) inthe high-k + metal gate transistors.

3.1. SRAM Cell 6T

Two CMOS inverters (M1, M2, and M3, M4) are coupled back-to-back in the SRAM memory bit-cell. As seen in Fig the word line (WL) controls the two pass transistors (M5 and M6), which are the access transistors. As long as the bit cell has power, it maintains one of two possible stable states: "0" or "1". Only when switching occurs does the SRAM cell consume current from the power source. Ideally, there is no static power dissipation when the device is idle. However, even when the SRAM is supplied with VDD, leakage power consumption at the deep sub micron (DSM) level in contemporary mobile processors is becoming an increasing concern. The data read sub cell is totally segregated from the data write mode. Further enhancing the stability of the cell is the total isolation of the data write sub-cell from

the data read sub-cell via BLs and vice versa.

1) Read Operation: As shown in Figure 2 the column and row decoders in which the data needs to be read decode SRAM cell addresses. It is first pre-charged to Vdd prior to the read operation begin. Upon activation of the word line (WL), it is discharged through the M5 transistor. Because of the cell driving current's restricted capabilities, the voltage change is relatively modest. The sense amplifier detects the slight voltage difference across s, and ultimately determines whether the value "1" or "0" is stored inthe SRAM cell.

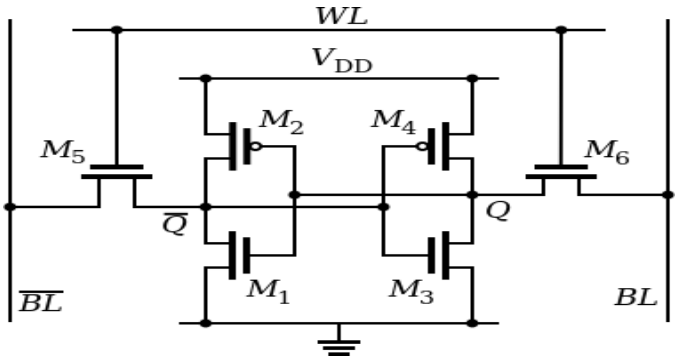

Figure 2 Six transistor (6T) SRAM cell

Write Operation: The data needs to be stored with the help of external devices. The address of the cell is provided by the column-row decoders. The write function, which is entirely dependent on the columngate condition, is executed to write the data into the cell when the WL is enabled. Because the write buffer is highly capable of driving the large driving current, the write operation takes less time than the reading operation requires.as shown in Figure 2.

3.2. SRAM Cell 7T

The primary purpose of the 7T-SRAM cell is to lower read and static power consumption. In this case, the transistor M7 is connected to provide a feedback mechanism that raises the primary inverter's high value and lowers the secondary inverter's value, and vice versa. By turning on WL, the M1 and M2 transistors execute the read and write operations, respectively. The M7 transistor is in the ON state during the read and the OFF state during the write operation. The performance of the read cycles is improved and the BLB (Read Bit-line) gets faster by resizing the M2 and M7 transistors. Figure 3 shows the configuration of the 7T-SRAM cell.

7T SRAM bit cells that use sleep mode to cut down on SRAM leakage power. Instead of silicon dioxide, a high-k gate dielectric material was used. The bit line pair utilized for the writing operations requires less discharge power because of the 7T cell. A highthreshold-voltage PMOS transistor is used as a extra sleep transistor. The sleep transistor's width is inversely connected with the voltage across the SRAM bit cell leakage, and the wake-up transistor and sleep transistor are paralleled, which lowers the sleep latency.

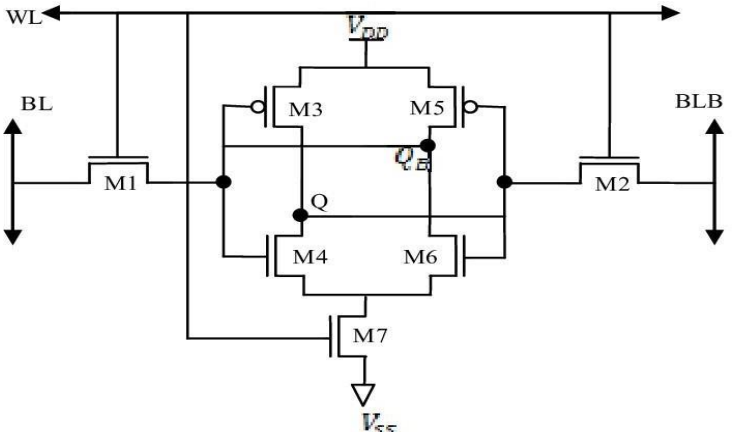

Figure 3 Seven transistor (7T) SRAM cell

3.3. SRAM Cell 8T

The schematic view of an 8T-SRAM cell is shown in Figure 4. The 8T-SRAM cell's structure is similar to that of a 6T SRAM cell, with the addition of two transistors (M7, M8) to serve as a barrier between the internal inverter and the WWL during read cycle operation. Prior to the read operation being initiated, the RBL is pre-charged to the supply voltage Vdd. Here, bit RWL enables reading, while bit RBL stays in one oftwo states—logic 1 or logic 0—depending on the QB internal node. The 8T-SRAM's write cycle is comparable to that of the 6T-SRAM.

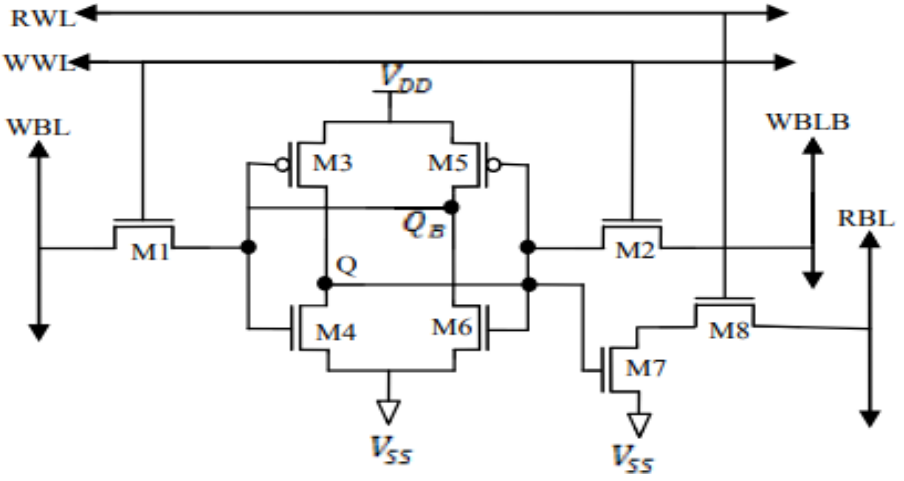

Figure 4 Eight transistor (8T) SRAM cell

3.4. 9T SRAM Design

The internal inverters are built using the pairs M4–M5 and M1–M3, and one bit of information is stored as shown in Figure 5. WB and transistor M2 have helped to complete the write cycle. Transistors M6, M7, and M8 are used in conjunction with bit RB to carry out the read cycle in the interim. The read cycle data stability has improved greatly as a result of the 9T structure.

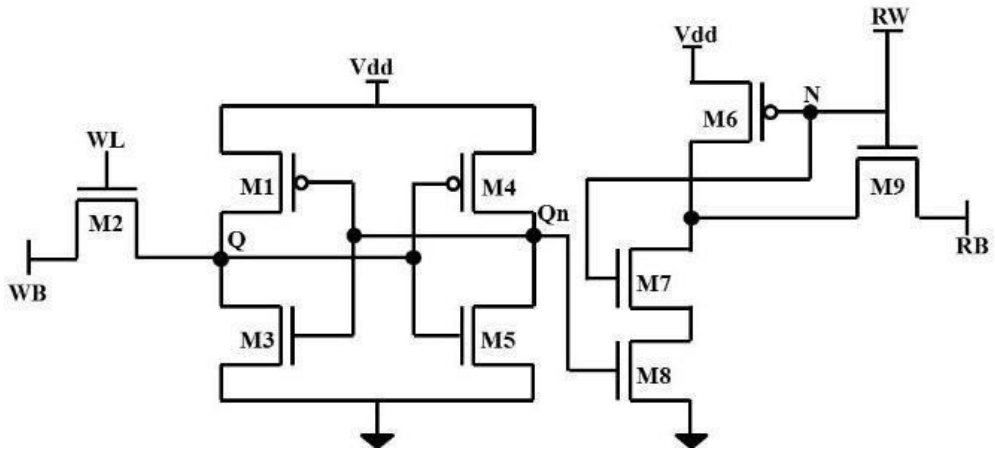

Figure 5 Nine transistor (9T) SRAM cell

Figure 6 shows a 10T SRAM cell. This circuit depicts the 10T SRAM Cell with differential read bit lines (BL and BLB). Two NMOS transistors (M7 and M9) are added to the 6T SRAM for the BL and the remaining two NMOS transistors (M8, M10) for the BLB. Pre-charge circuits need to be placed on the BL and BLB in addition to the 8T SRAM.

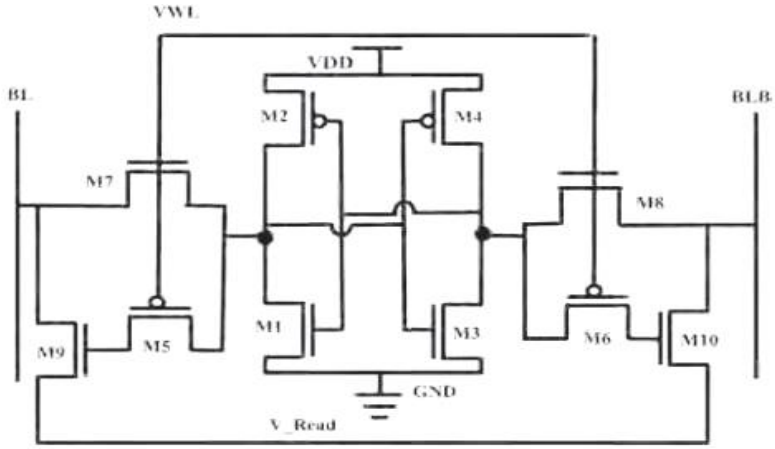

Figure 6 Ten transistor (10T) SRAM cell

4. Results and Discussion

Low power consumption is the ultimate aim in VLSI circuits. To achieve this, we have to measure the power consumption of different SRAM cells and this can be held by parameter P_{avg}. Another important parameter is delay which shows the time taken by the SRAM cells to produce the outputs from input bit-lines. If we achieved less amount of delay, then the SRAM cells will be operated in high-speed.

Schematics and simulation results of read and write operation of 6T,7T,8T,9T,10T is as indicated in Figure 7,8,9,10, 11.

4.1. 6T SRAM Cell

6T SRAM Cell Simulation has been done on tanner EDA tool using technology called "Generic_025", which represents a standard, 0.25um CMOS process as depicted in Figure 7.

4.1.1. Read Operation

Let us assume that the data stored at Q in the memory is a 1. Precharging both bit lines to a logical 1 and then asserting the word line WL to enable both access transistors initiates the read cycle. The second phase is when the transistor M4 charges itself as it turns on since Q is logically set to 0, or when the {Q<BLB} approaches Vdd, a logical 1. Conversely, the opposite would occur and BL would be pulled towards 1 and BL towards 0 if the memory's contents were a 0. At that point, the voltage across these BL and ~BL will be higher, indicating whether or not 1 was the read operation speed.

4.1.2. Write Operation

The value to be written is applied to the bit lines at the beginning of a write cycle. To write a zero, we would apply a zero to the bit lines, which would mean setting BL to 0 and ~BL to 1. By inverting the bit line values, a 1 is written. The value to be stored is then latched when WL is asserted. Note that the bit line input drivers' design makes them far stronger

than the cell's comparatively weak transistors, allowing them to easily override the cross-coupled inverters' previous state, which is why this works. An SRAM cell's transistors must be sized carefully in order to ensure proper operation.

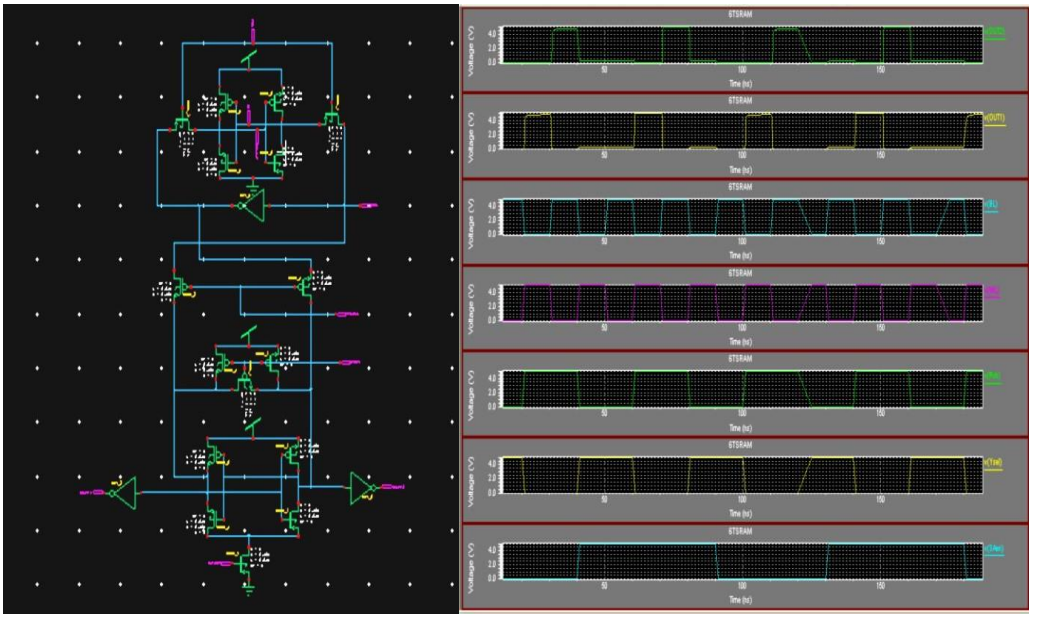

Figure 7 Schematic & Simulation of 6T SRAM

4.2. 7T SRAM Cell

Figure 8 shows 7T SRAM Cell .When '1' stored in cell, M3 and M2 are ON and there is

positive feedback between ST node and STB node, therefore ST node pulled to V_{dd} by M2 and STB node pulled to GND by M3. When '0' stored in cell M4 is ON and since N node maintained at V_{dd} by M5 the STB pulled to V_{dd}, also M2 and M3 are OFF and for data retention without refresh cycle following condition must be satisfied. For satisfying above condition when '0' stored in cell, we use leakage current of access transistors (Ml), especially sub-threshold current of access transistors (MI). For this purpose during idle mode of cell, bit-line maintained at GND and word-line maintained at V Idle.

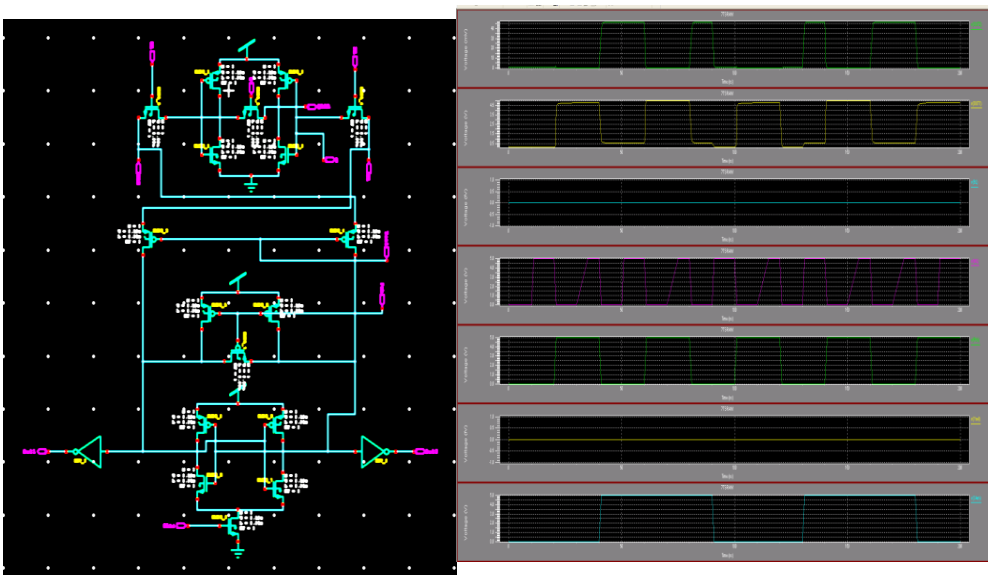

Figure 8 Schematic & simulation of 7T SRAM

4.3. 8T SRAM Cell

In Figure 9 ,8T SRAM cell is shown, Four transistors N1, N2, P1, P2 form a cross-couple structure to store data. Four transistors P3 and N3- N5 are access to the internal nodes D and /D of the cell. N3 and N4 connect the cell internal nodes D and /D of the cell. N3 and N4 connect the cell internal nodes to the BLs while P3 and N5 form an inverter to control the voltage of node C1. The source terminal of P3 is connected to a column select (CS) line while gates of P3 and N5 are connected to WL. Unlike conventional design, the sources of P1 and P2 are connected to dynamic cell supply (cell supply) line which is raised to the higher voltage during read operation to obtain a higher noise margin.

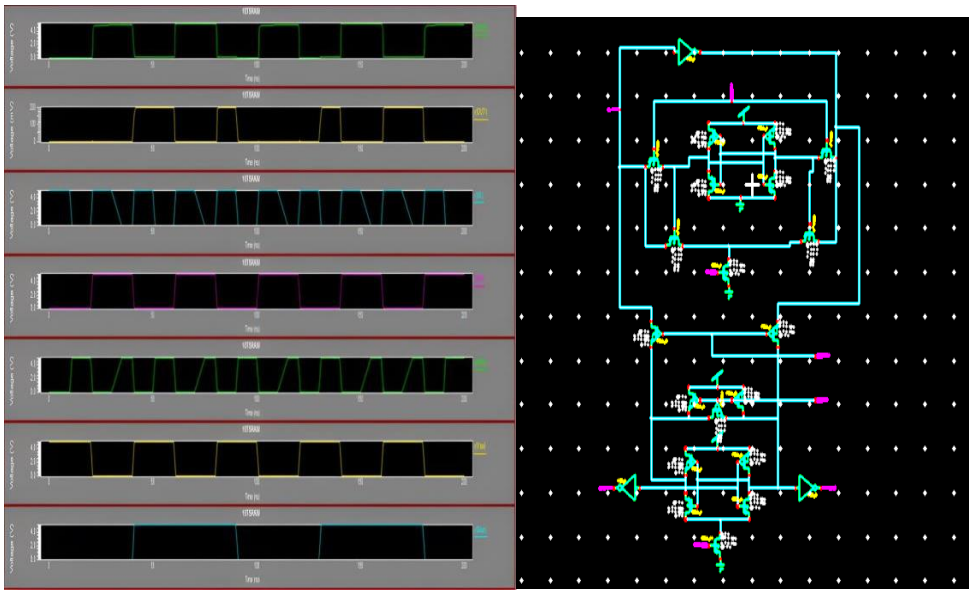

Figure 9 Schematic & Simulation of 8T SRAM High K Metal

4.4. 9T SRAM Cell

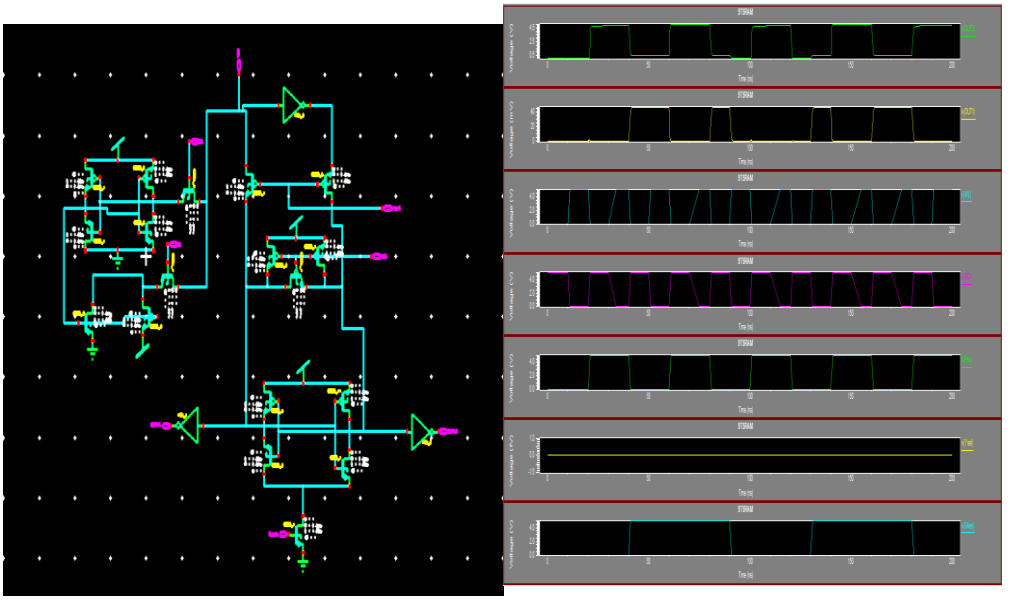

Figure 10 Schematic & Simulation of 9T SRAM High K

4.5. 10T SRAM Cell

The 10T SRAM cell is depicted in Figure 11. The 10T SRAM Cell with differential read bit lines (BL and BLB) is shown in this circuit. The 6T SRAM has two NMOS transistors (NMOS_4 and NMOS_8) connected for the RBL and two more NMOS transistors (NMOS_6 and NMOS_7) for the BLB. Pre-charge circuits need to be put on the BL and BLB in addition

to the 8T SRAM.

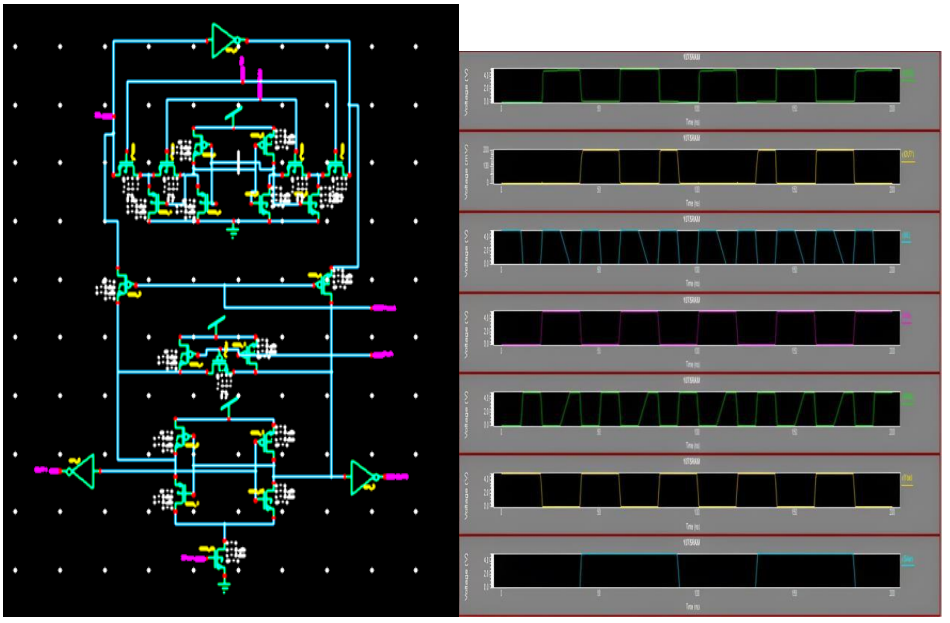

Figure 11 Schematic & Simulation of 10T SRAM High K Metal

Power consumption comparison is carried out for different SRAM cells. The design implementation of the SRAM with High K and Bulk CMOS of 8T Transistor is more effective compared to other type of SRAM Cell.and it is as shown in Table II.

Table II Power Comparison with High K and Bulk CMOS Design

Type of SRAMCell	Power Consumed (Watts)		Delay Time	
	Bulk	High K	Bulk	High K
6T	2.529862e-010	2.313557e-010	1.40604e-007	6.06062e-008
7T	4.290068e-010	4.149817e-010	1.8e-007	1.8e-007
8T	2.778079e-010	2.660088e-010	1.60876e-007	1.60827e-007
9T	3.346793e-010	3.326007e-010	8.1e-008	1.61e-007
10T	4.656154e-010	4.507464e-010	1.8e-007	1.4e-007

4.6. Physical Layout Deign of 8T SRAM

A schematic's physical form is called a layout. For the physical mask layout creation, a set of geometric constraints or regulations specific to a given manufacturing process must be adhered to. The electrical characteristics of the devices and the design guidelines relevant to the related manufacturing process define the geometries. The functionality and performance specifications of the cell to be developed come first in the mask layout design of a CMOS logic gate or cell, and the layout comes last. The transistor's initial size and circuit architecture are included in the specs. The tanner EDA tool are used to simulate the designed transistor level schematic and the layout is drawn for 8T SRAM as shown in Figure 12.

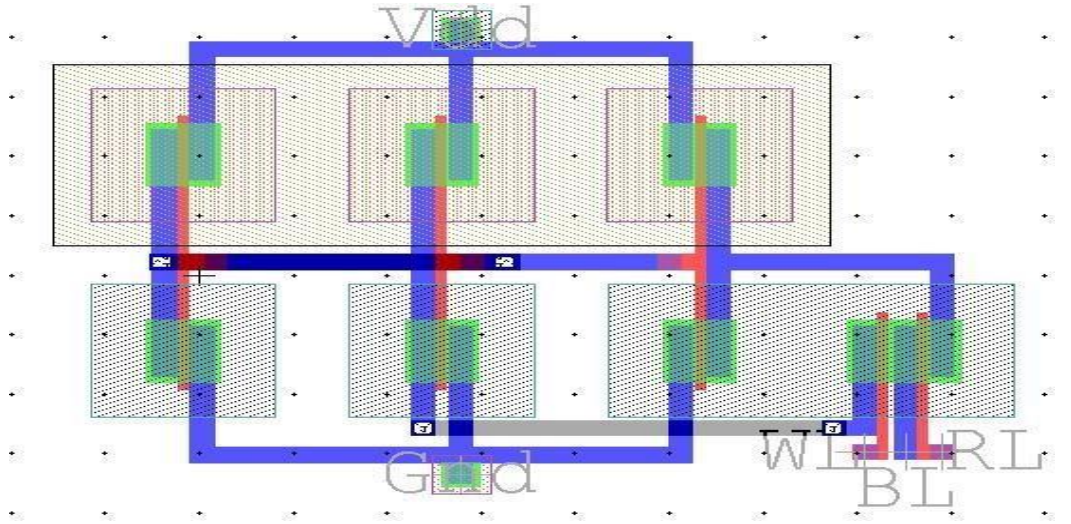

Figure 12 8T SRAM Layout

5. Conclusions

This research explores low-power SRAM design techniques in detail, with an emphasis on applications where energy efficiency is critical. When high-k metal is effectively utilized, it minimizes leakage current, uses less power, and improves the transistor's overall speed performance when compared to bulk CMOS.DRAM is quicker than SRAM and is dynamic whilst SRAM is static. Cheaper DRAM is utilized in main memory, whereas SRAM is frequently used in cache memory. It is more expensive than DRAM and utilizes more transistors per bit of memory than DRAM. It requires less power than DRAM.

Overcoming the limitations of SiO_2, High-k metal gate (HKMG) technology has become the industry standard in semiconductor fabrication today. When combined with metal gates, high-k material such as compounds based on hafnium are frequently employed as gate dielectrics, giving greater control over the transistor and facilitating the creation of smaller, more effective devices.

References

1. Kavitha, S.; Kumar, C.;Fayek, H.H.; Rusu, E. Design and Implementation of CNFET SRAM Cells by Using Multi-Threshold Technique. Electronics 2023, 12, 1611.https://doi.org/10.3390/electronics12071611.
2. Xue, X.; Sai Kumar, A.;Khalaf, O.I.; Somineni, R.P.;Abdulsahib, G.M.; Sujith, A.;Dhanuja, T.; Vinay,M.V.S. Design and Performance Analysis of 32 _ 32Memory Array SRAM for Low-Power Applications. Electronics 2023, 12, 834. https://doi.org/10.3390/electronics12040834.
3. Renren Xu; Jiaxin Yao; Gaobo Xu; Yanzhao Wei; Huaxiang Yin; Qingzhu Zhang; Guoliang Tian; Yanrong Wang; Gangping Yan; Jinjuan Xiang; Weihai Bu; Yongqin Wu; Zhenhua Wu; Jun Luo; Wenwu Wang Experimental Investigation of Ultrathin Al_2O_3 Ex-Situ Interfacial Doping Strategy on Laminated HKMG Stacks via ALD IEEE Transactions on Electron Devices April 2022.

4. Y. -J. Yao et al., "SiGe/Si Superlattice Ferroelectric HfZrO2 ΩFET and CMOS Inverter With SSmin,n =62.4 mV/dec, ION/IOFF > 1.0 × 107, and Voltage Gain = 111.4 V/V," in IEEE Electron Device Letters, vol. 45, no. 2, pp. 260-263, Feb. 2024, doi: 10.1109/LED.2023.3331741.
5. C. Gastaldi et al., "Ferroelectric Junctionless Double-Gate Silicon-On-Insulator FET as a Tripartite Synapse," in IEEE Electron Device Letters, vol. 44, no. 4, pp. 678-681, April 2023, doi: 10.1109/LED.2023.3249972.
6. H. Kim et al., "Effect of ALD Processes on Physical and Electrical Properties of HfO2 Dielectrics for the Surface Passivation of a CMOS Image Sensor Application," in IEEE Access, vol. 10, pp. 68724-68730, 2022, doi: 10.1109/ACCESS.2022.3183593.
7. N. Liu et al., "HfO_2-Based Ferroelectric Optoelectronic Memcapacitors," in IEEE Electron Device Letters, vol. 44, no. 3, pp. 524-527, March 2023, doi: 10.1109/LED.2023.3235909.
8. Erfan Abbasian, Shilpi Birla, Ashish Sachdeva & Elangovan Mani (25 Jul 2023): A low-power SRAM design with enhanced stability and ION/IOFF ratio in FinFET technology for wearable device applications, International Journal of Electronics, DOI: 10.1080/00207217.2023.2238326.
9. N. Shylashree, M. S. Amulya, Gulur R. Disha, N. Praveena, Vijay Kumar Verma, S. Muthumanickam, V. Kannagi, K. Sivachandar & Vijay Nath (07 May 2023): A Novel Design of Low Power & High Speed FinFET Based Binary and Ternary SRAM and 4*4 SRAM Array, IETE Journal of Research, DOI: 10.1080/03772063.2023.2207549.
10. C. Gastaldi et al., "Ferroelectric Junctionless Double-Gate Silicon-On-Insulator FET as a Tripartite Synapse," in IEEE Electron Device Letters, vol. 44, no. 4, pp. 678-681, April 2023, doi: 10.1109/LED.2023.3249972.
11. H. Kim et al., "Effect of ALD Processes on Physical and Electrical Properties of HfO2 Dielectrics for the Surface Passivation of a CMOS Image Sensor Application," in IEEE Access, vol. 10, pp. 68724-68730, 2022, doi: 10.1109/ACCESS.2022.3183593.
12. N. Liu et al., "HfO_2-Based Ferroelectric Optoelectronic Memcapacitors," in IEEE Electron Device Letters, vol. 44, no. 3, pp. 524-527, March 2023, doi: 10.1109/LED.2023.3235909.
13. Erfan Abbasian, Shilpi Birla, Ashish Sachdeva & Elangovan Mani (25 Jul 2023): A low-power SRAM design with enhanced stability and ION/IOFF ratio in FinFET technology for wearable device applications, International Journal of Electronics, DOI: 10.1080/00207217.2023.2238326.
14. N. Shylashree, M. S. Amulya, Gulur R. Disha, N. Praveena, Vijay Kumar Verma, S. Muthumanickam, V. Kannagi, K. Sivachandar & Vijay Nath (07 May 2023): A Novel Design of Low Power & High Speed FinFET Based Binary and Ternary SRAM and 4*4 SRAM Array, IETE Journal of Research, DOI: 10.1080/03772063.2023.2207549.
15. Vijay Kumar Sharma (2021): A survey of leakage reduction techniques in CMOS digital circuits for nanoscale regime, Australian Journal of Electrical and Electronics Engineering, DOI: 10.1080/1448837X.2021.1966957.
16. M. V. Nageswara Rao,Mamidipaka Hema,Ramakrishna Raghutu,Ramakrishna S. S. Nuvvula,Polamarasetty P. Kumar,Ilhami Colak,and Baseem Khan (07 Jun 2023) : Design and Development of Efficient SRAM Cell Based on FinFET for Low Power Memory Applications Hindawi Journal of Electrical and Computer Engineering Volume 2023, Article ID 7069746, 13 pages https://doi.org/10.1155/2023/7069746.
17. John Robertson Robert M Wallace (Volume8 February 2015) : High-K materials and metal gates for CMOS applications ELSEVIER
18. D. Nirmal, P. Vijayakumar, P. Patrick Chella Samuel, Binola K. Jebalin & N. Mohankumar (2013) Subthreshold analysis of nanoscale FinFETs for ultra low power application using high-k materials, International Journal of Electronics, 100:6, 803-817, DOI:10.1080/00207217.2012.720955