

Analysis and Design of Efficient High Voltage Gain Interleaved Boost Converter for Solar PV System

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To optimize the power output of the PV array, it is recommended to employ a high-gain interleaved dc-dc boost converter in the PV energy conversion system. The proposed converter builds upon the existing two-phase interleaved dc-dc boost converter, which is commonly used in utility grid integration circuits or high-power applications due to its ability to minimize ripple current from the PV. The primary objective of this research project is to elevate the output voltage of the currently installed PV array in order to cater to high-power applications or grid integration. The key requirements include achieving high-efficiency power conversion and fully utilizing the potential of the PV system. While previous methods have been proposed to increase the solar source's output voltage, they suffer from drawbacks such as low efficiency, complexity, and cost. In contrast, the suggested dc-dc converter boasts a remarkable efficiency of 96% and is capable of converting voltage from 25V to 400V for a power output of 400W. The performance of the proposed converter topology has been validated through MATLAB simulation.

Keywords: PV System, DC-DC converter, high gain, soft switching, interleaved boost converter.

1. Introduction

The photovoltaic system is widely recognized as a solution to modern energy challenges due to its clean and renewable nature, making it well-suited for electricity distribution. However, efficient transmission of PV energy to the load requires a high-efficiency interface. This article introduces a two-stage switched capacitor and linked inductor high boost interleaved boost converter, which aims to enhance the efficiency of solar power generation systems using MPPT technology. Compared to other dc-dc converter circuits, this converter achieves

significant voltage gain at a low duty ratio, resulting in reduced voltage stress across switches, decreased conduction loss, and minimized ripple. The integration of a two-stage switching capacitor with a connected inductor effectively boosts the voltage gain, while a passive clamp circuit enables zero voltage switching of primary switches and zero current switching facilitated by the intrinsic loss of the inductor. By regulating the current drop rate through leakage inductance, the converter mitigates issues related to reverse recovery of the diode, ultimately leading to increased efficiency. Renewable energy sources, such as PV, have gained increased attention from experts in response to the global energy crisis. Although PV is widely used in everyday life, its energy conversion system suffers from poor conversion efficiency and unpredictable source availability. To address these challenges, a high step-up DC-DC converter is employed to elevate the low voltage profile of PV. This converter finds applications in various fields, including automotive headlights, Uninterruptible Power Systems (UPS), and communication power systems. However, conventional converter topologies experience increased voltage stress on switches when dealing with high step-up voltages, leading to reduced effectiveness and failure to meet application requirements.

Numerous converter topologies have been proposed to achieve high step-up voltage gain. The DC-DC flyback converter, while featuring a simple structure and high voltage gain, experiences significant voltage stress on switches due to leakage inductance. Energy-regeneration strategies have been applied to mitigate this stress. The phase-shifted full-bridge converter, on the other hand, generates higher input ripple currents and achieves a high step-up gain by utilizing a higher number of turns ratio in the transformer. Electrolytic capacitors are employed in the phase-shifted full-bridge converter to reduce input current ripples.

Switching capacitor-based converter circuits, such as active-clamp dual boost and active-clamp full bridge boost converters, are also used to achieve high step-up conversion with high efficiency. However, these converters suffer from drawbacks such as high transient current and substantial conduction loss in the switch, as well as increased complexity with more switched capacitor cells. Soft-switching techniques have been introduced in switched-capacitor cell designs to reduce switching loss and electromagnetic interference. Additionally, a coupled inductor approach with modified turns ratio is utilized to achieve a large step-up gain. Nevertheless, all currently used high step-up ratio converters and ultra-step-up converters still experience significant voltage stress across the diode.

The primary drawbacks of the PV energy conversion system lie in its poor energy conversion efficiency and the unpredictable nature of climate conditions. To maximize the power output of PV, it is essential to operate at the maximum power point, prompting the development of several MPPT control algorithms. This paper focuses on the design and operation of an improved two-phase interleaved boost converter topology, covering voltage stability analysis and simulation results. Furthermore, it discusses features such as automatic current sharing, reduced voltage stress on switches and diodes, and overall increased efficiency in various chapters.

2. Proposed Topology

The proposed high voltage high gain interleaved dc-dc Fig. 1 depicts the suggested interleaved high voltage, high gain dc-dc boost converter for high step-up conversion with MPPT control.

.Where,

- L_1, L_2 - Magnetizing Inductances
- D_1, D_2, D_3, D_4 - Clamp diodes
- C_1, C_2 - Clamp capacitors
- C_3, C_4 - Output capacitors
- S_1, S_2 - Main Switches

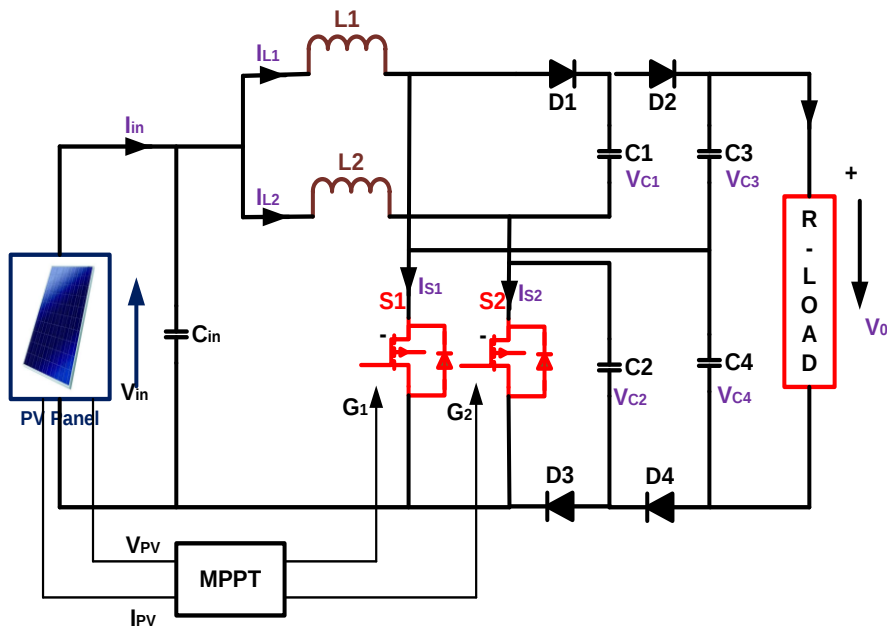


Figure 1: Proposed High Voltage gain DC-DC Converter

The fundamental interleaved boost converter is expanded upon in the proposed converter architecture by the addition of two extra capacitors and diodes. The energy held in the inductor and capacitors, along with the energy of the other capacitor, is transferred to the output during the energy transfer period, allowing the proposed converter to achieve voltage gain twice. Comparatively to a traditional interleaved two-phase boost converter, active switches and diodes experience less voltage stress. The integrated MPPT controller maximises conversion rates while monitoring maximum power. When the duty cycle is greater than 0.5, a continuous conduction mode of operation is used to produce the high voltage gain. High voltage gain and current sharing capabilities are not achievable when the duty ratio is less than 0.5 and the operating mode is discontinuous conduction. because the inductor, blocking capacitor, and capacitor are not transferring enough energy to one

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another.

(i) Mode 1: ($t_0 \leq t < t_1$)

In this setting of functioning. The diodes D1, D2, D3, and D4 are switched OFF while switches S1 and S2 are turned ON. Fig. 2 depicts the current's flow. Current flow increases i_{L1} and i_{L2} , and the energy stored in the inductors L1 and L2 increases. Diodes D4 and D2 clamping voltages are equal to $(V_{C4} - V_{C2})$ and $(V_{C3} - V_{C1})$, and diodes D1 and D3 clamping voltages are equal to V_{C1} and V_{C2} of the capacitor voltage, respectively.

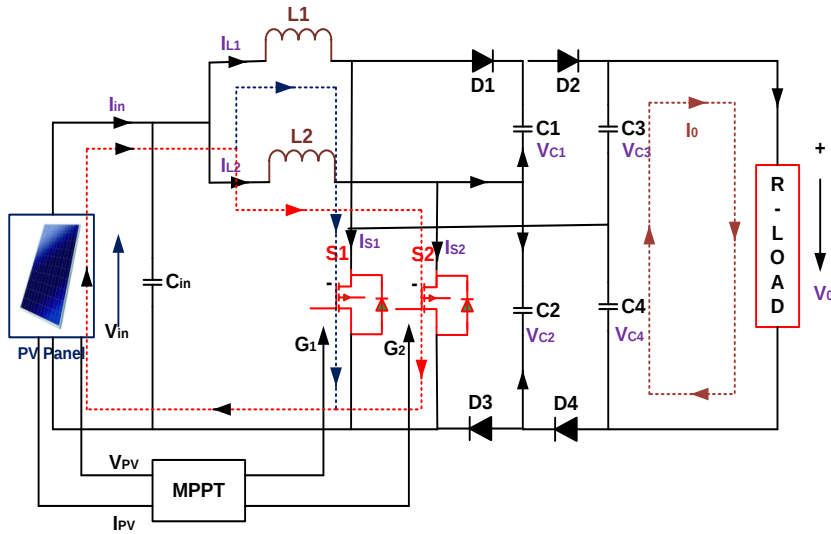


Fig 2: Operating circuit of Mode-1

Capacitors C3 and C4 supply power to the load. The voltage across the capacitors is given below.

$$V_{in} = L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} \quad (1)$$

$$C_1 \frac{dV_{c1}}{dt} = C_2 \frac{dV_{c1}}{dt} = 0 \quad (2)$$

$$C_3 \frac{dV_{c3}}{dt} = C_4 \frac{dV_{c4}}{dt} = -\left(\frac{V_{c3} + V_{c4}}{R}\right) \quad (3)$$

(ii) Mode 2: ($t_1 \leq t < t_2$)

Switch S2 is turned OFF for the duration of the pause. Diodes D2 and D3 are still conducting, as is switch S1. Fig. 3 depicts the current flow. Energy is stored in capacitor C1 and released into capacitor C3 of the output capacitor by inductor L2. Energy from the inductor L2 is stored in C2. In this mode, the inductor current i_{L2} falls linearly and the capacitance-voltage $V_{C3} = V_{C2} + V_{C1}$ rises constantly.

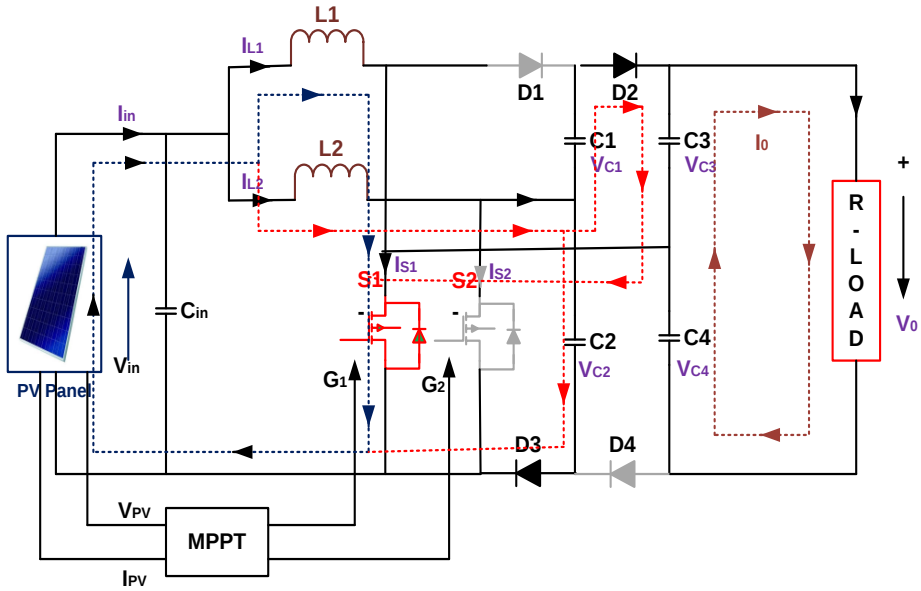


Fig 3: Operating circuit of Mode-2

The various voltage components in this mode is given below.

$$V_{in} = L_1 \frac{di_{L1}}{dt} \quad (4)$$

$$V_{in} - V_{c2} = L_2 \frac{di_{L2}}{dt} \quad (5)$$

$$C_1 \frac{dV_{c1}}{dt} = I_{C2} - I_{L2} \quad (6)$$

$$C_2 \frac{dV_{C2}}{dt} = I_{C1} + I_{L2} \quad (7)$$

$$C_3 \frac{dV_{C3}}{dt} = -I_{C1} - \left(\frac{V_{c3} + V_{c4}}{R} \right) \quad (8)$$

$$C_4 \frac{dV_{C4}}{dt} = - \left(\frac{V_{c3} + V_{c4}}{R} \right) \quad (9)$$

(iii) Mode 3: ($t_2 \leq t < t_3$)

The switches S1 and S2 are switched ON and function similarly to mode 1 during this mode of operation.

(iii) Mode 4: ($t_3 \leq t < t_4$)

The switch S2 is turned ON and kept in the OFF position when in this mode of operation. D1 and D4 were retained in an ON state as well.

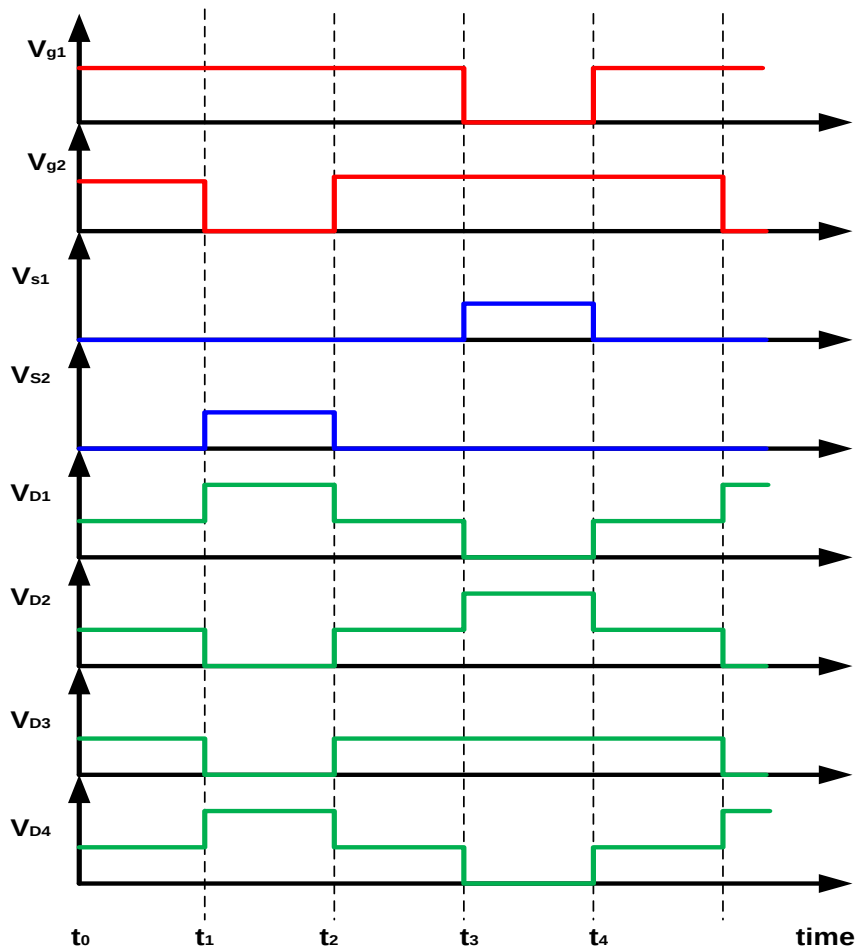


Figure 4: Operating waveforms

As the load and the output capacitor C4 approach, the stored energy in the inductor L1 and capacitor C2 is released. VC4=VC2+VC1 is the voltage across the output capacitor. While inductor current iL2 constantly grows, iL1 drops linearly.

$$.L_1 \frac{di_{L1}}{dt} = V_{in} - V_{C4} + V_{C2} = V_{in} - V_{C1} \quad (10)$$

$$V_{in} = L_2 \frac{di_{L2}}{dt} \quad (11)$$

$$C_1 \frac{dV_{C1}}{dt} = i_{C2} + i_{L1} \quad (12)$$

$$C_2 \frac{dV_{C2}}{dt} = i_{C1} - i_{L1} \quad (13)$$

$$C_3 \frac{dV_{C3}}{dt} = -\left(\frac{V_{C3} + V_{C4}}{R}\right) \quad (14)$$

$$C_4 \frac{dV_{C4}}{dt} = -i_{C2} - \left(\frac{V_{C3} + V_{C4}}{R}\right) \quad (15)$$

The suggested converter's symmetrical mode of operation makes implementation simple. Additionally, the functional waveforms in Fig. 4 depict minimal voltage stress and uniform current distribution in active switches and diodes.

3. Voltage Stress Analysis

The capacitor voltage ripple is taken to be zero for the purposes of more straightforward analysis. Below is a direct calculation of the voltage stresses across the active switches S1 and S2.

$$DV_{in} + (1-D)(V_{in} - V_{C1}) = 0$$

and

$$DV_{in} + (1-D)(V_{in} - V_{C2}) = 0 \quad (16)$$

The capacitor voltage V_{C3} and V_{C4} are,

$$V_{C3} = V_{C1} + V_{C2} = \frac{2}{1-D} V_{in}$$

and

$$V_{C4} = V_{C1} + V_{C2} = \frac{2}{1-D} V_{in} \quad (17)$$

The output voltage is,

$$V_0 = V_{C3} + V_{C4} = \frac{4}{1-D} V_{in} \quad (18)$$

Duty ratio,

$$M = \frac{V_0}{V_{in}} = \frac{4}{1-D} \quad (19)$$

The voltage stresses across the switches S1 and S2

$$V_{S1} = V_{S2} = \frac{1}{1-D} V_{in} \quad (20)$$

The voltage stress on power switches is,

$$V_{S1} = V_{S2} = \frac{V_0}{4} \quad (21)$$

The voltage stress across the power switches is equivalent to one-fourth of the output voltage, as shown by Equation 21. Therefore, the proposed converter can handle power conversion with low-voltage rating devices. Conduction and switching losses are thereby significantly decreased.

4. Simulation Results

The proposed converter's performance is confirmed for a 400W rating using the MATLAB simulation model. The suggested converter converts the input voltage of 25V to the output voltage of 400V. For both switches S1 and S2, a uniform duty ratio of 0.75 and a switching frequency of 40 Hz are used. The input ripples are lessened by the interleaved mode of operation. Increasing the switching frequency reduces the size of inductors and output ripples.

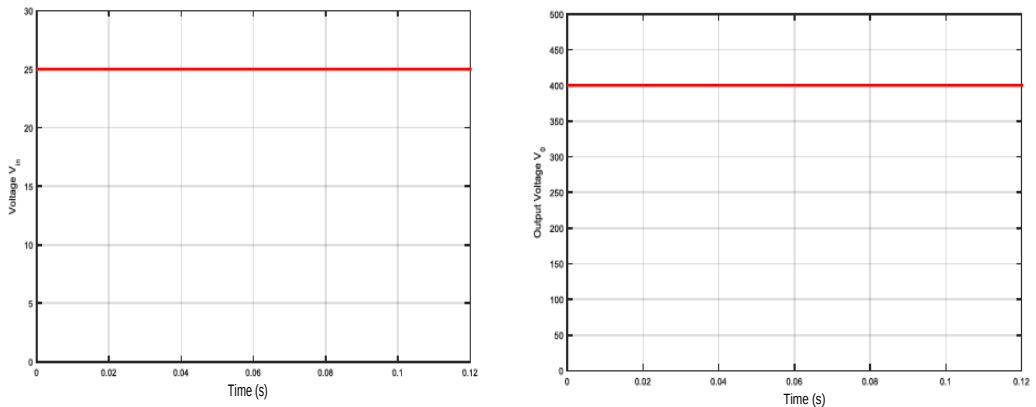


Figure 5 Input and output Voltage

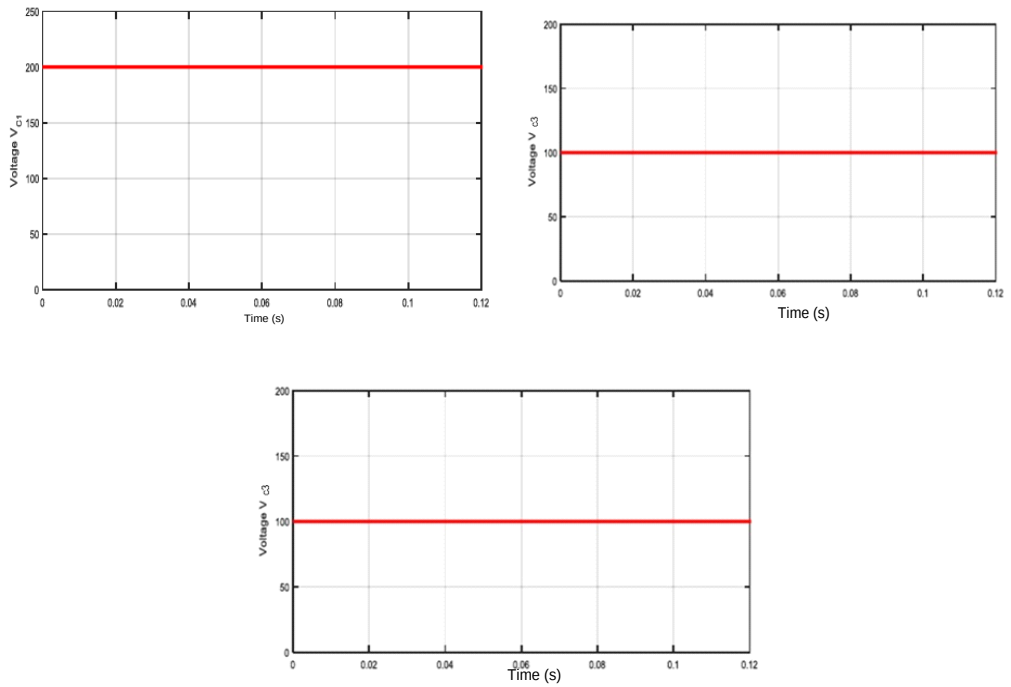


Figure 6 Results obtained for blocking capacitor & Output capacitor

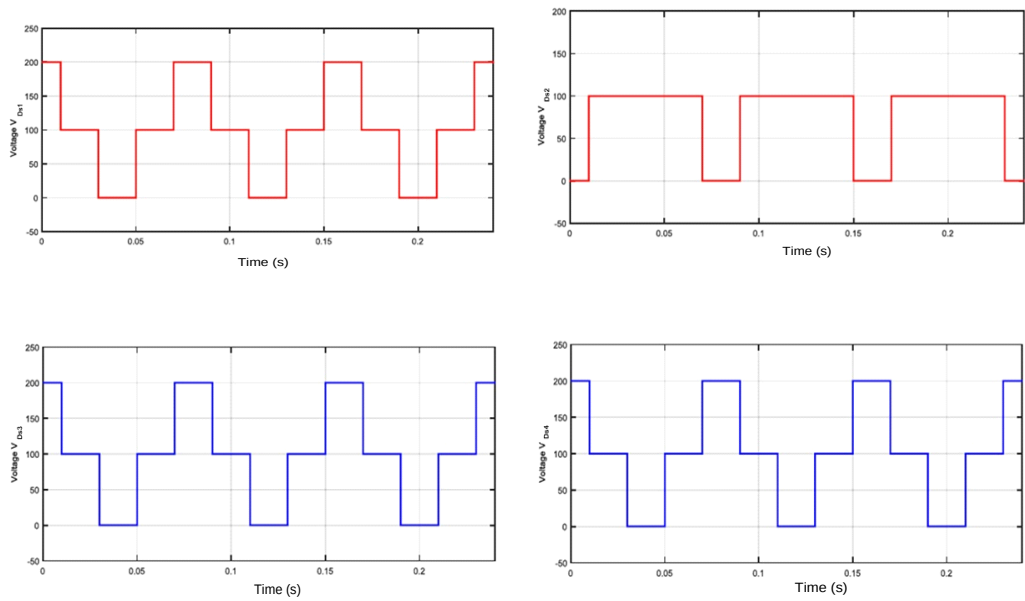


Figure 7 Voltage stress on VDS1, VDS2, VDS3, VDS4.

Fig. 5 displays the proposed circuit's input and output voltages. Figure 6 displays the output capacitor voltage waveform and the blocking capacitor voltage waveform. The voltage stress across the active switch is depicted in Fig. 7. The suggested converter's reduced voltage stress across the switches and diodes efficiently lowers the corresponding losses and raises efficiency.

5. Performance Analysis

The proposed topology and the methods mentioned in the literature are compared in terms of performance in table 1. The voltage gain and normalised voltage stress for active switches are displayed in Table 1.

Table 1 Comparison of voltage gain and voltage stress of proposed converter with other converters

	Voltage gain			Voltage stress		
Duty Ratio	0.5	0.6	0.7	0.5	0.6	0.7
Voltage Doubler	4	5	6	0.5	0.5	0.5
High Step Up Ratio Converter	5	6.1	7	0.4	0.43	0.45
Proposed Converter	8	10	14	0.25	0.25	0.25

Fig 8 shows the comparison of the characteristic curve and fig 9 shows the normalized voltage stress comparison of the proposed and conventional topologies.

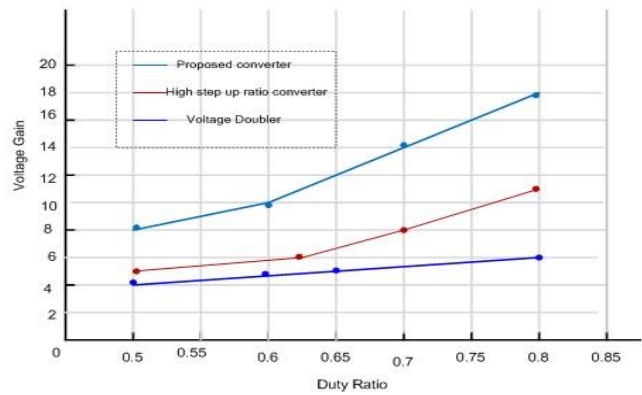


Figure 8. Voltage gain

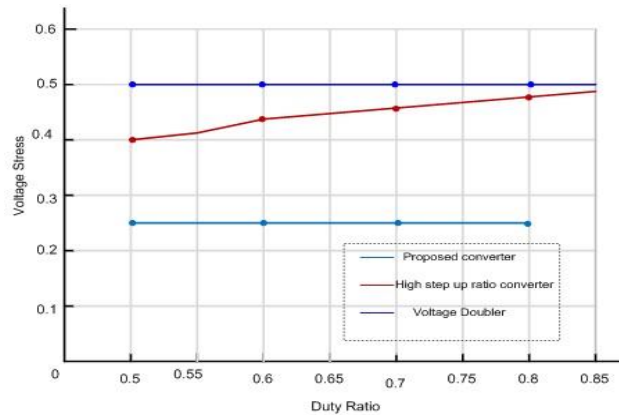


Figure 9. Active Switches Normalized Voltage Stress

Figures 8 and 9 compare the characteristic curves of the proposed and traditional topologies using normalised voltage stress.

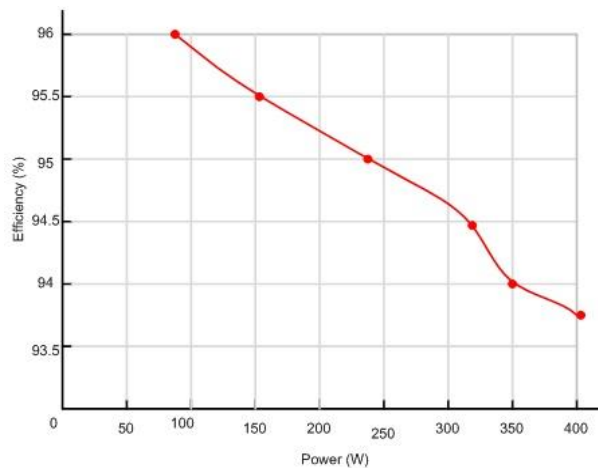


Figure 10 Proposed Converter Efficiency

Fig. 10 illustrates the proposed converter's MPPT-assisted 96% maximum efficiency. The power produced by the proposed converter with an MPPT control is 2.4 times larger than that of the converter without an MPPT control.

6. Conclusions

This study examined a high-gain interleaved dc-dc boost converter for PV systems using an MPPT controller. High voltage gain is achieved while maintaining a low duty cycle. Both conduction and switching loss are decreased by the low voltage stress. Another benefit is the ability to share current symmetrically without building any additional circuits. The power transmission level is raised by the proposed converter and MPPT controller. The total outcome demonstrates that the proposed converter is better suited for applications requiring

substantial step-up voltage gains.

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