

Experimental and Numerical Investigation of Solder Joint Reliability of Ball Grid Array Package under Board level Drop Test

Y. Venkata Naga Chandana, Venu Kumar Nathi

*Department of Mechanical Engineering, GITAM School of Technology, Telangana, India.
Email: chandana.svn@gmail.com*

Portable microelectronic devices have become lighter and thinner, enhancing their portability. However, this increased portability also raises the risk of accidental drops, which can cause significant damage to these devices. To address this issue, the Joint Electronic Device Engineering Council (JEDEC) has formulated a board-level drop test standard to improve the reliability of portable microelectronic devices. In this research paper, experiments were conducted on a printed circuit board (PCB) measuring 100x100x1mm, with Ball Grid Array (BGA) Package assembled centrally, to evaluate the performance of the package during impact loading. Experiments were conducted under five different service conditions specified by JESD22-B111. Drop tests were also simulated using the Input-G method in explicit dynamic analysis conducted with ABAQUS software. The resulting strain and impact pulse data from both the experiments and simulations were compared to validate the accuracy of the simulated model. Dynamic responses of the board obtained from simulations under service condition B, which involves an impact pulse of 1500G and for a duration of 0.5 milliseconds was comprehensively studied to understand the solder joint failure under impact loading. The study also examines the impact of moisture on the reliability of solder joints during drop impact by conducting drop-to-failure experiments on moist and baked PCBAs. Weibull's probability distribution plots were used to compare the reliability of BGA Package under moist and baked conditions.

Keywords: Ball Grid Array Package, Explicit dynamic analysis, Impact loading, Input-G method, Printed circuit Board.

1. Introduction

The Electronic products frequently encounter shock and vibration during transportation, handling, and accidental drops during regular use. The trend towards higher functional density and increased use of chip-scale packages (CSPs) has resulted in electronic components being placed closer to product housings, increasing their vulnerability to drop damage. Portable devices, in particular, need to endure multiple drops, and the smaller pads and solder joints resulting from decreased I/O pitch make drop reliability more challenging. A significant concern is solder joint failure, which arises from a combination of PCB bending and mechanical shock when subjected to drop. Drop testing was simulated in explicit dynamic analysis using input G method for different configurations of PCB and Packages to evaluate the dynamic responses and also correlated experimentally. [1,2,3,4,5] Chang-Lin Yeh et al utilized a support excitation strategy integrated with an implicit time integration technique to study the transient structural behavior of a board-level chip-scale package subjected to consecutive drop impacts. The research focused on examining the cumulative stresses, plastic deformations, and plastic strain energy densities within the solder joints due to repeated drop impacts. [6] Meng-Kao Yeh and Tzu-Heng Huang used support excitation method in Finite element methods to study the drop impact of a FR-4 test board and correlated the results of full and quarter model with that of experiments. [7] An emphasize on different methodologies of explicit finite element modelling which would reduce the computational time yet produce reliable results like, smeared property models, Timoshenko-beam element models, explicit sub-models, reduced integration element formulations, continuum-shell models were used to study fatigue life behaviour of solder joints under thermal cycling and shock impact and also validated against the experimental results. [8,9,10,11] The fatigue life of lead-free solder joint during drop tests is analysed and predictive fatigue life model for solder alloys is established using Physics of Failure (PoF) approach. [12] Robert Darveaux et al evaluated and compared the reliability of different lead-free solder alloys under various testing conditions, including solder joint array tensile tests, cyclic bend tests, thermal cycle tests, drop testing, and temperature cycling using Weibull statistical analysis. [13] Life of solder joints under the influence of substrate technology and solder ball composition during drop tests was studied and their relative drop test performance was assessed by Weibull analysis. [14] Guozheng Yuan conducted drop tests and stated that the main failure mode during shock impact is pad cratering, and that the solder joint might not be the weakest part of the assembly. [15] C.Y. Zhou explored the dynamic response of common portable electronic devices subjected to drop impact loading and utilized a Hopkinson bar in a dynamic test rig to measure the resulting impact force pulses. [16] Behaviour of multi-layered multi-materials PCB model which is suitable for high-speed and high-frequency applications is evaluated under drop impact, both through numerical and testing. [17,18] The strain energy density obtained from the simulations was used as the primary criterion for evaluating the performance of the solder joints in the drop tests. [19,20,21] A parametric analysis of the Printed Circuit Board Assembly (PCBA) was conducted, considering variables such as PCB thickness, PCB modulus, underfill material, solder ball height, solder ball pitch, and mounting hole position. [22,23,24,25] David Cadge performed a system level drop test for a cordless optical computer mouse using sub modelling techniques in Abaqus software which is an effective way to look at small details

in a larger model. [26] E. Tempelman presented an experimental and analytical study on the dynamic behaviour during impact of portable products with internal shock mounting. [27] The impact of moisture content on crack formation in Ball Grid Array (BGA) components during reflow soldering was studied, highlighting the need for effective moisture management in semiconductor packaging processes. [28] Qiu et al. studied how temperature, vibration, moisture, and dust impact BGA solder joint reliability, highlighting their role in causing stress, fatigue, and corrosion. [29] Experiments were conducted to understand the moisture sensitivity of the materials and optimize the package design to mitigate the effects of moisture to ensure the reliability and integrity of packages. [30] Samuel Ambosta studied the effect of humidity on thermal cycling of BGA packages through simulation and experiments. Also, made detailed comparison on deformation, stresses and strains in normal thermal cycling against thermal cycling with humidity. [31] Timothy. P investigated moisture-induced degradation of interfacial adhesion in microelectronic assemblies, to prevent premature package failures. [32]

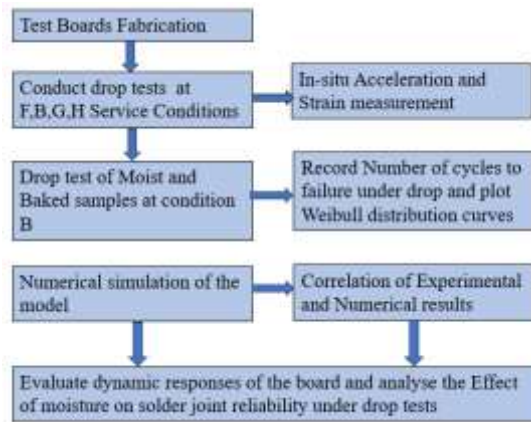


Figure1: Flow chart of the research process

To build confidence in the simulated model and facilitate design improvements, it is essential to validate the simulation against experimental results. Figure 1 indicates the flow of research in this paper. In this study, experiments were conducted to achieve the desired impact pulse by adjusting the drop height, and the strain in the PCB board was measured. The same test was also simulated, and the results were compared. Dynamic responses of the PCB which is a key parameter to understand the failure of the solder joint is studied in detail through the simulated results. Additionally, this paper examines the impact of moisture and the effectiveness of baking on drop impact performance, utilizing Weibull probability distributions to analyse the results.

2. Methodology

2.1. Test Model

In this study, we assess the reliability of a 96-TWBGA (Thin Wafer Ball Grid Array)

package through drop testing. The BGA measuring 9mm x 13mm is centrally mounted on a 100x100x1mm PCB. The BGA is equipped with 96 solder balls, each 0.5mm in diameter and spaced at 0.8mm pitch, facilitating daisy-chained solder joint failure identification. The resistance readings of daisy-chain test sample before and after the test (after each drop) are measured. When the resistance reading exceeds 1000 ohms, it is considered a failure. If possible, in situ resistance measurement is preferred, because the solder joint crack induced during the impact may close-up again, or in partial contact after the test. For partial solder joint failure, the resistance reading usually is less than 10 ohms. Once the solder joint fails or open completely, the resistance reading should be many orders higher, usually in the range of M-ohms. Consistent testing procedure and failure criteria are required to produce same level of acceleration and impact life results with high repeatability. The PCB has 3.1mm diameter mount holes at the four corners to facilitate mounting in the drop table. The placement of the BGA at the centre of the PCB ensures maximum deflection during drop tests, focusing our evaluation on the reliability of solder joints in this critical location. [4] Figure 2 illustrates the schematic drawing of the BGA, while Figure 3(a) depicts the schematic drawing of the PCB used as the test model designed using KiCAD software. Figure 3(b) presents the test board after assembling the BGA on the PCB. Table 1 shows the specifications of the BGA and the PCB considered for the study.

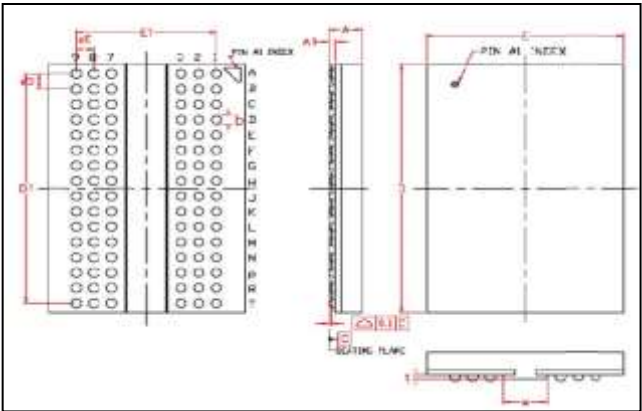


Fig. 2 Schematic diagram of 96 ball BGA

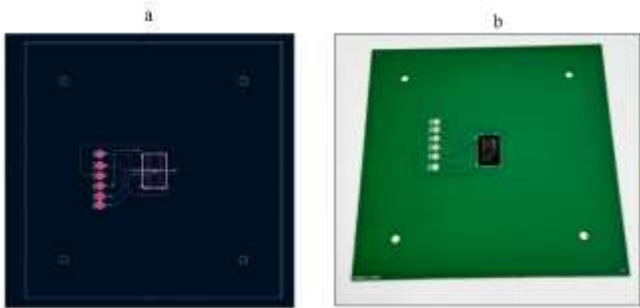


Fig. 3 (a) Schematic drawing of the test board (b) Actual Test Board

2.2. Experimental Setup

The evaluation performance of Printed Circuit Board Assembly (PCBA) and the failure of solder joints under drop impact was conducted in accordance with the standard JESD22-B111A. [33] This research involves a drop test using Lansmont P-30 shock test tower. The drop table used had dimensions of 30x30 cm and capable of achieving a maximum acceleration of 5000G. The test board with the components facing upwards, was mounted on a base plate (135x135x25 mm) using four standoffs with a diameter of 3.1 mm, and the base plate was rigidly fastened to the drop table. To achieve the required impact pulse, the height of the drop table was adjusted using the lifting mechanism of the drop test tower. The drop table was then released freely via the guide rods to hit the strike surface with the impact. The impact impulse was delivered to the drop table in the form of a half sine wave. A single-axis shock accelerometer was attached to the base plate to measure the acceleration pulse generated upon impact. Also, two CEA-XX-125URA model rectangular strain gauge rosettes were attached to the PCB on the component side—one near the BGA and the other near a standoff—to measure longitudinal strain at the centre and corner of the PCBA during the drop event. Figure 4(a), 4(b), 4(c), 4(d) shows the shock test tower, strain gauges bonded on PCBA, drop table and PCBA mounted on the base plate respectively. The data from the strain gauges and the accelerometer were captured and processed using National Instruments Data Acquisition (NI-DAQ) hardware and LabVIEW software respectively. Upon impact, the drop table experiences an acceleration pulse in the form of a half sine wave, whose equation is given by

$$A(t) = A_0 \sin\left(\frac{\pi t}{t_w}\right) \quad (1)$$

where A_0 is the G level, at the given service condition and t_w is time of impact set to 0.5 ms. The amplitude of the shock pulse may be obtained from the drop height from the equation

$$A_0 = \frac{\pi\sqrt{2gH}}{t_w} \quad (2)$$

Where g is the acceleration due to gravity 9.8m/s^2 and H is the drop height and t_w is time of impact.

2.2. Test conditions

The experiments were conducted at five different service conditions of G values, mentioned in Table 1, by adjusting the drop heights. Maximum and minimum principal strain and acceleration data were captured using the Data Acquisition Cards.

Table 1. JEDEC service conditions for board level drop test

Test Condition	Impact Pulse (G)	Drop Height(m)	Impact time (ms)
F	900	0.8	0.7
B	1500	0.9	0.5
G	2000	1.1	0.4
-	2500	1.3	0.4
H	2900	1.5	0.3

3. Finite element model for Impact analysis

Several validated methods were developed to simulate drop impacts. Researchers have used both implicit and explicit dynamics to simulate drop tests. One challenge in modelling the shock response of electronic products is the significant variation in the dimensions of individual layers, such as solder interconnects, copper pads, and chip interconnects, compared to the overall size of the PCB assembly. This discrepancy necessitates a fine mesh to accurately model the chip interconnects while simultaneously capturing the system-level dynamic behaviour, which makes the computational effort highly demanding. Explicit dynamic analysis tends to provide more accurate results during the short duration of the impact pulse. The simulation time is dictated by the size of the time step, which is directly proportional to the length of the smallest element in the model [34]. Studies were carried out wherein the PCBA was modelled using various elements such as conventional shell elements, tetrahedral elements, and hexagonal elements. These models have then been validated against experimental results. [9] Additionally, modelling solder balls as beam elements was proposed to reduce computational time. [11] In this paper Input-G method was chosen for comparison against experiments conducted under different service conditions outlined by JESD22-B111. As this standard numerical drop test is expected to yield consistent and realistic results. [4]. In this method impulse pulse obtained from the experiments is directly given to the mount point avoiding the guide rods, drop table and strike surface as in actual drop test. A complete model of the printed circuit board assembly (PCBA) was created for the simulation, with the BGA modelled as per the dimensions provided in the component datasheet. The BGA package was modelled with the substrate, underfill, and die sequentially, with the die encapsulated within the overmold. The PCB measures 100x100x1 mm and has 3.1 mm diameter mount holes, with the BGA assembled centrally, as shown in Figure 5(a). The dimensions and material properties of the components are given in Table 3. The BGA consists of 96 solder balls, each with a diameter of 0.5mm and a pitch of 0.8mm as shown in Figure 5(b). Figure 5(c), 5(d) shows the BGA and solder balls respectively. Figure 6 shows the components of PCBA. The solder balls were modelled with copper pads on both sides of the interface with the package and the PCB. The current simulation uses a linear elastic material model for the sake of simplification. As a result, the current model only requires basic mechanical properties like modulus, density, and Poisson's ratio.

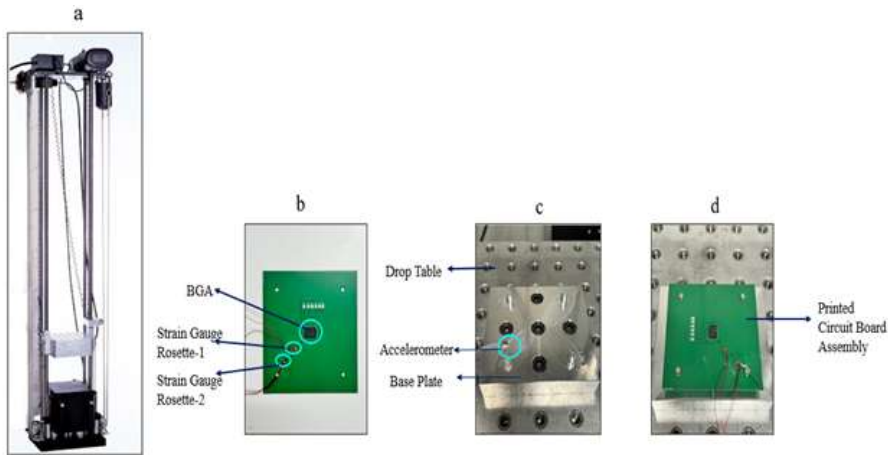


Figure 4 (a) Shock Test Tower used to conduct the experiment (b) Strain gauge rosettes stuck on PCBA (c) Base plate and Drop table (d) PCBA mounted on Base Plate

Table 2. Specifications of BGA and PCB

Specifications of BGA								
Size	Solder diameter	ball	Pitch of solder balls	Number of solder balls	Over mold thickness	Solder material	ball	Substrate thickness
9mmx13mm	0.5mm		0.8	96	1.5mm	Sn63pb 37Eutectic		0.75mm
Specifications of the PCB:								
PCB material	No of layers	Surface Finish	FR-4 -TG	Thickness	Track Spacing	Finished copper		
FR-4	2	HASL with lead	TG150-160	1mm	6/6mil	1OZ Cu		

Table 3. Dimensions and Material Properties

	PCB	Solder ball	Copper pad	Substrate	underfill	Silicon	Overmold
Dimension (mm)	100x100x1thick	0.5diameter	0.5 diameter 0.02thick	0.75	0.02	0.75thick	1.5
Youngs Modulus (GPa)	20	50	160	20	10	130	25
Poisons Ratio	0.3	0.3	0.3	0.3	0.3	0.3	0.3
Density(kg/m ³)	1780	860	8830	1850	1500	2230	2040

3.2. Mesh and boundary conditions

Reduced integration method and first order equations were utilized in the analysis because they require fewer integration points to form the element stiffness matrices, thereby reducing computational time for simulating transient dynamic events. First-order elements are more effective when large strains or very high strain gradients are anticipated, as is common in impact scenarios [9]. Higher-order elements exhibit higher frequencies compared to lower-order elements, which can generate noise when stress waves propagate through an FE mesh. Consequently, lower-order elements are more suitable for modelling a shock wave front. PCB, solder balls and component were modelled with reduced integration solid elements. Mesh transition at the interface of solder ball-package and solder ball-PCB was obtained through Tie constraint. The assembly employed C3D8R elements throughout, totaling

148,610 nodes and 108,622 elements. Boundary conditions specified an impact pulse in terms of acceleration G with component facing upwards, applied to the mount holes positioned at the PCBA's four corners. This pulse, following JESD22-B111 standard testing conditions, consisted of a half-sine wave in the Z-direction, lasting 0.5 milliseconds. The simulation was carried for a 10ms, impact impulse being given at the 0.5ms. A linear bulk viscosity parameter of 0.06 was considered which determines damping coefficient at high impact pulses.

4. Effect of Moisture in Drop Testing

In this paper experiments were conducted to investigate the effect of moisture under shock loading. This study aims to assess the effect of humidity on the reliability of solder joints under drop test. Controlled experiments were conducted on two sets of samples. The first set, comprising seven samples, was placed in a humidity chamber as shown in Figure 6 maintained at 60% relative humidity (RH) for 168 hours to ensure adequate moisture absorption. The second set of seven samples underwent a baking process at 120°C for 10 hours to remove any absorbed moisture. Following these treatments, both sets of samples were subjected to drop tests to evaluate their performance. By comparing the results, the study aims to determine how moisture can affect the mechanical integrity and durability of the PCBAs under impact stress.

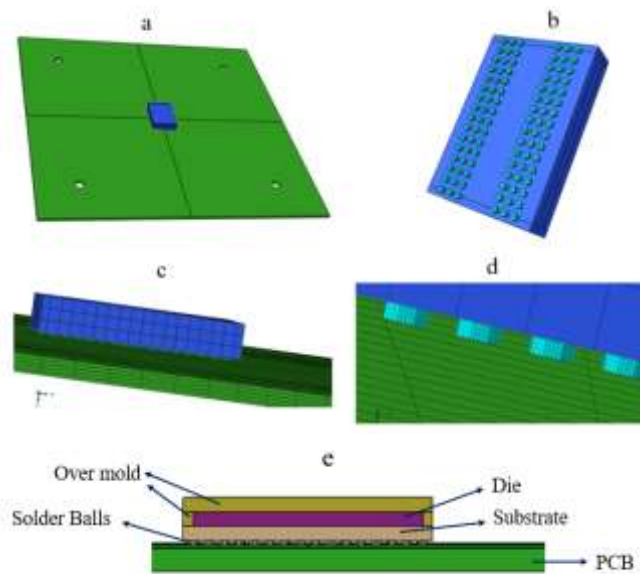


Fig. 5 a) PCBA b) BGA c) Detailed View of assembled BGA on PCB (d) BGA Solder ball PCB interface (e) Components of the assembly



Fig. 6 Samples placed in Humidity chamber

To investigate the effect of moisture on the reliability of the BGA package, an event detector was employed to continuously monitor the resistance of the daisy-chained circuits during the testing process. This setup allowed for real-time detection of resistance changes, which are indicative of failure events. The event detector recorded the number of drops each sample endured before failure, providing precise data on the durability and reliability of the BGA packages under moisture conditions. The number of drops-to-failure for each sample was recorded, and Weibull probability distribution curves were drawn and analyzed. This analysis helps to understand how moisture exposure impacts the mechanical integrity and performance of BGA packages during drop impact tests.

5. Results and Discussion

5.1. Correlation of experimental and Numerical Results

The impact pulse generated by dropping the drop table from various specific heights was measured using an accelerometer attached to the drop table. These heights are adjusted to bring about service conditions as mentioned under JEDEC standard. To ensure repeatability, the impact pulse was recorded three times for each specific height as Drop-1, Drop-2, Drop-3 in Figures 7(a) to 10(a), illustrate the impact pulses measured for different drop heights, showing the variations in pulse intensity. Rectangular strain gauge rosettes were attached to the PCB—one near the center and another near a mounting hole—to measure longitudinal strain of the PCB during each drop. The strain captured by the strain gauges is compared with simulated results obtained from Input-G method. Figure 7(b), 8(b), 9(b), 10(b) and 11 (b) shows the comparison of experimental and simulated strain. There exists a close correlation between the measured and simulated strain of the PCB. This comparison helps validate the accuracy of the simulation model. When the drop table abruptly comes to rest from a free-fall condition, it generates an acceleration pulse in the direction opposite to the drop. This acceleration pulse is transmitted to the PCB through the four screws that fasten

the PCB to the drop table. Despite the drop table’s sudden stop, the PCB, due to inertia, continues to move downward except at the points where it is fastened to the drop table. The PCB then rebounds and oscillates up and down until the vibrations subside due to its inherent structural damping. Therefore, it can be inferred that in a free-fall drop impact process, the failure of solder joints is caused by a combination of the sudden acceleration pulse transmitted to the PCB and the resulting bending action of the PCB. Table 4 presents the maximum principal strain measured experimentally near the BGA and the mounting hole, along with the corresponding simulated results.

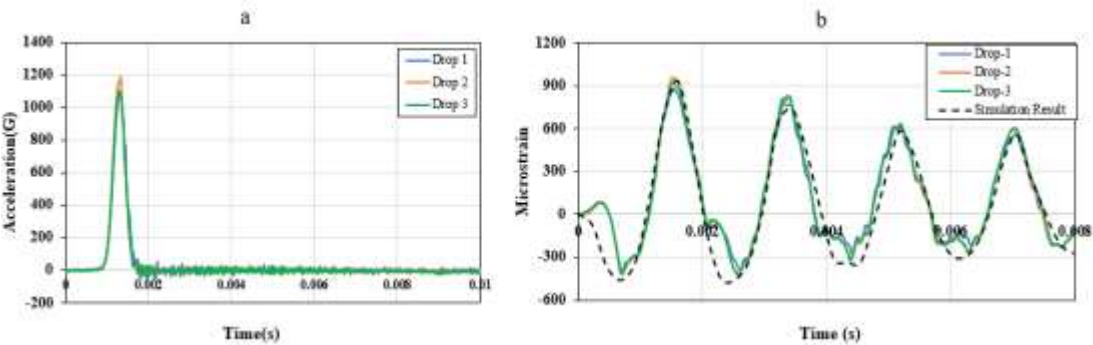


Fig. 7 (a) Impact Pulse drop height 0.8m (b) comparison of experimental and simulation at 900G.

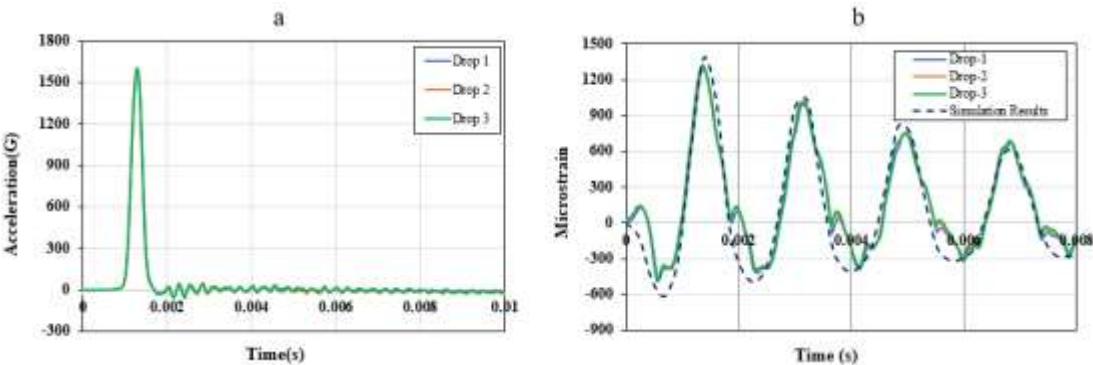


Fig. 8 (a) Impact Pulse drop height 0.9m (b) comparison of experimental and simulation at 1500G.

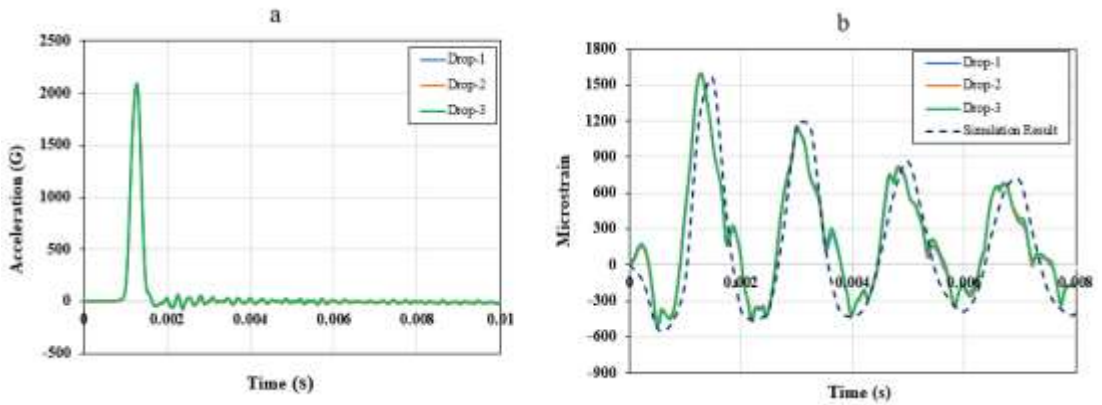


Fig. 9 (a) Impact Pulse drop height 1.1m (b) comparison of experimental and simulation at 2000G.

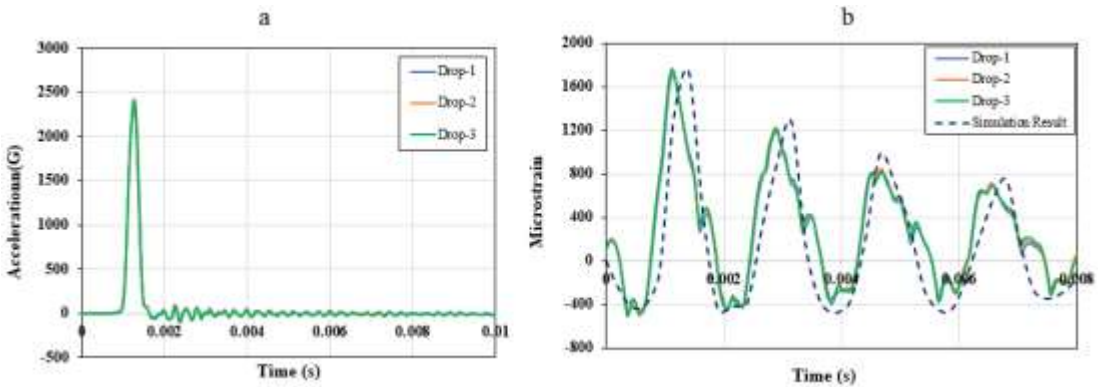


Fig. 10 (a) Impact Pulse drop height 1.3m (b) comparison of experimental and simulation at 2500G.

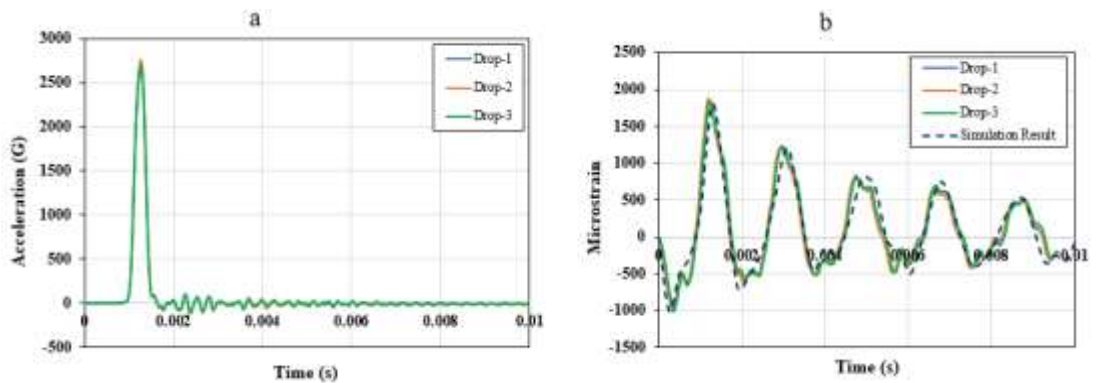


Fig. 11 (a) Impact Pulse drop height 1.5m (b) comparison of experimental and simulation at 3000G.

The percentage error between the experimental and simulated data shows a maximum deviation of 6%, indicating a high level of accuracy in the simulation. This small error margin demonstrates that the simulation is in excellent agreement with the experimental results, thereby validating the reliability of the simulated model. Consequently, this validated model can be confidently used as an alternative to physical experiments for evaluating dynamic responses and conducting parametric analyses.

Table 4. Comparison of Experimental and Simulated Maximum Principal Strain

Test condition	G	Maximum Principal Strain Measured near the BGA		% error	Maximum Principal Strain Measured near Mount Hole		% error
		Experimental	Simulation		Experimental	Simulation	
F	900	946.2	928.9	1.82	877.63	843.2	3.92
B	1500	1304.7	1384.7	-6.13	1285.4	1305.6	5.76
G	2000	1601.8	1545.2	3.53	1578.9	1536.7	2.67
-	2500	1707.7	1749.6	-2.45	1677.6	1698.1	1.22
H	3000	1927.8	1805.8	6.32	1885.9	1856.8	1.54

5.2. Dynamics responses of the PCB from Input G Method

With the validated FEA model established, the dynamic responses of the PCBA under service condition B with impact pulse 1500G for a duration of 0.5ms and BGA facing upwards has been comprehensively understood by analyzing the results obtained from the simulation. This condition was chosen for its relevance to typical impact scenarios that portable microelectronic devices might encounter. This study allows for accurate prediction of the PCB’s behavior under impact conditions, enabling detailed insights into stress distribution, deformation patterns, and potential failure points, facilitating improvements in design and material selection to enhance durability and reliability. Figure 12 demonstrates the deflection characteristics of the PCB during upward and downward bending caused by sudden impact. Upon impact the PCB exhibits upward bending, generating compressive stresses in the solder balls as shown in Figure 12(a), and Figure 12(b) illustrates the downward bending of the PCB which induces tensile stresses in the solder balls. Figure 13(a) indicates the deflection measured at the center and near mount hole of the PCB. The analysis reveals that the maximum deflection during downward bending is 1.616mm, located at the PCB center, while the maximum deflection during upward bending is 1.485mm at the same location. The least deflection is observed at the mounting holes as PCB is fixed at the standoff. It is understood that maximum deflection occurs at a duration of 0.5ms and PCB bending diminishes thereafter. Figure 13(b) illustrates the strain distribution in the corner most solder joint which is the critical joint experiencing maximum strain in the simulated result. Figure 13(b) displays the maximum principal strain, normal strain in the x-direction (LE11), and vertical normal strain (LE33) as derived from the simulation results. The results reveal that LE33 exhibits the highest strain values, while LE11 presents the lowest. Figure 14(a) depicts the stress in the array of solder balls and Figure 14(b) shows the Maximum stress developed in the corner most solder ball of the BGA. Figure 15(a), (b) presents the Maximum Principal stress, normal stress in the x-direction(S11), and vertical normal stress

(peel stress, S33) in both the corner most solder joint and solder ball at the center of the BGA respectively. The peel stress (S33) emerges as the most significant stress in both cases. However, the magnitude of S33 is 94.43MPa in the corner most joint, compared to 10MPa in the solder ball at the center of BGA, indicating that corner joints are more vulnerable. Therefore, the peeling stress becomes a critical factor during drop impact and serves as a key failure criterion for design optimization. Since peeling stress is primarily induced by PCB bending or vibration, it can be inferred that PCB bending is the major failure mechanism for the PCB assembly under drop impact. Figure 16 provides a comparative analysis of the stresses in both the corner most and centrally located solder joint of the BGA, quantifying the differences in stress magnitudes.

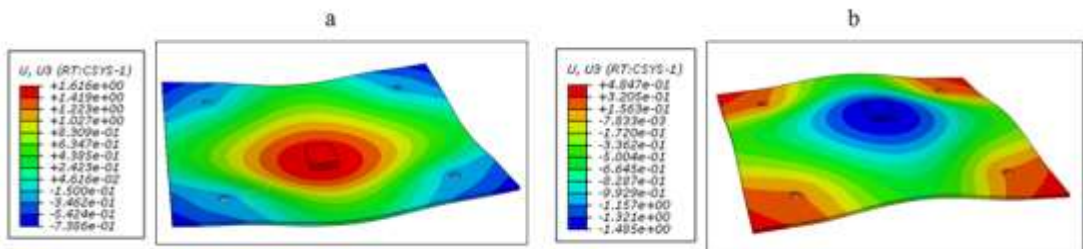


Fig. 12 Deflection in PCBA (a) PCBA bending upwards (b) PCBA bending Downwards

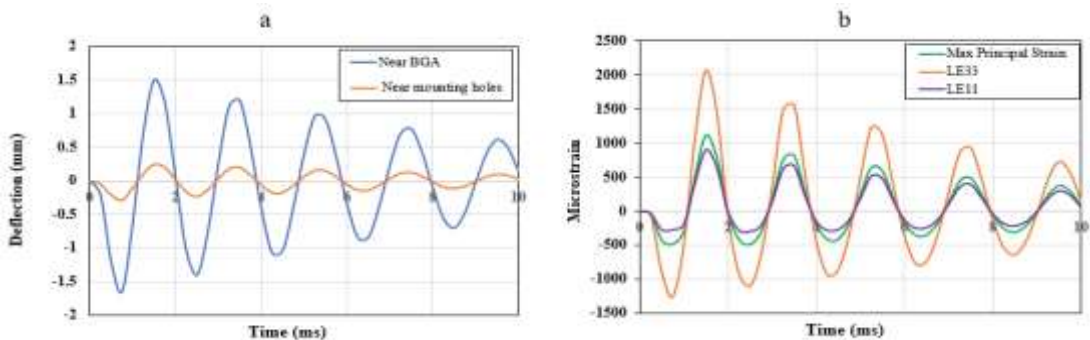


Fig. 13 (a) Deflection in the PCBA (b) Strain in the critical solder ball

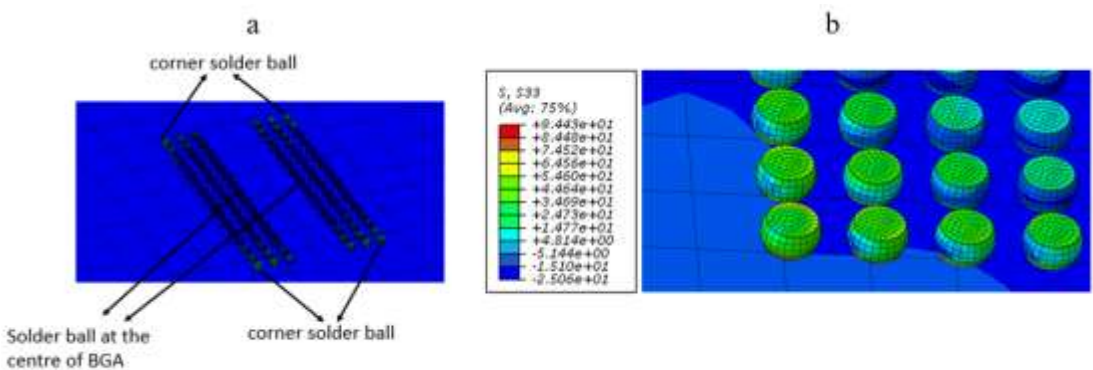


Fig. 14 (a) Stress in Array of solder balls (b) Stress in corner solder ball

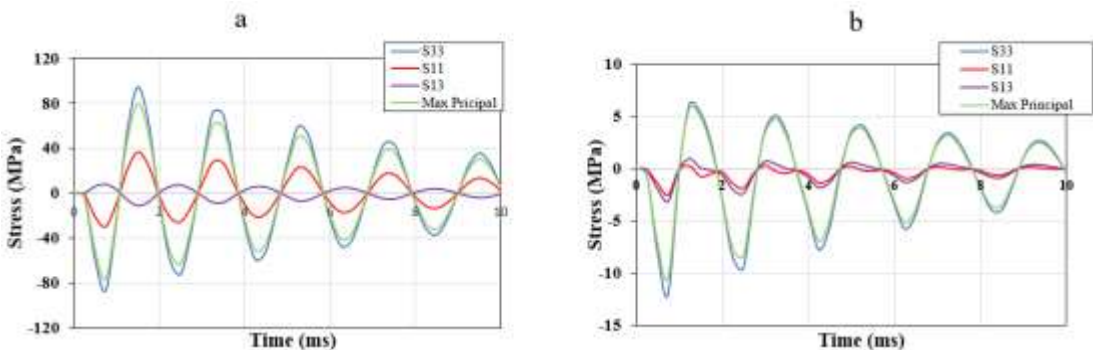


Fig. 15 Dynamic Stresses in (a) Corner solder ball (b) Solder ball in the center of BGA

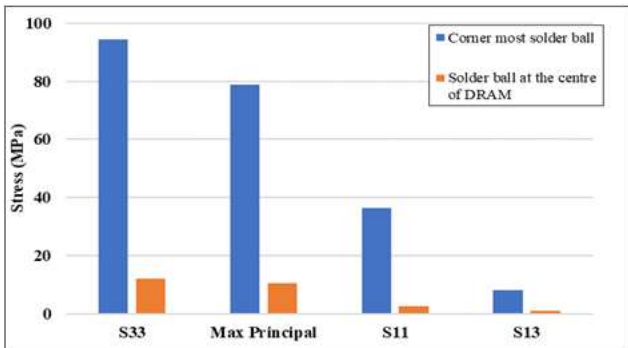


Fig. 16 Comparison of stresses in corner most solder ball and solder ball at the center of BGA

5.3. Effect of Moisture in Drop testing

Drops-to-failure of moist and baked samples obtained through the experimentation were analyzed statistically using Weibull’s probability distribution plot. Figure 18, illustrates the relationship between the number of drops to failure and the cumulative percentage of failure

for both moist and baked samples. Key reliability metrics, such as the Mean Time to Failure (MTTF) and B10 life, are also indicated in the Figure 18. The MTTF for the baked samples is approximately 22 drops, whereas for the moist samples, it is around 8 drops. The B10 life, which denotes the number of drops at which 10% of the samples have failed, is 17 drops for the baked samples and 5 drops for the moist samples. This data clearly indicates that the moist samples, which absorb moisture and gain weight, are significantly more susceptible to failure during drop impact compared to the baked samples. Further, the shape and scale parameters for both sets of samples, generated using JMP software are detailed in the Table 5. The shape parameter offers insights into the distribution and failure rates of the samples, while the scale parameter highlights the characteristic life. For the baked PCBAs, the Weibull shape parameter (β_0) was estimated at 7.744, indicating a pronounced increasing failure rate over time. This suggests that the failure rate for baked PCBs accelerates as the components age. In contrast, for the moist PCBs, the shape parameter (β_1) was estimated at 4.861, which signifies that baked PCBAs are more consistent and have a predictable failure distribution compared to moist PCBAs. The scale parameter (η_0) for baked PCBs was estimated at 21.132, signifying a relatively longer characteristic life before failure. The scale parameter (η_1) for moist PCBs was 8.441, indicating a shorter characteristic life. These findings reveal that while both types of PCBs exhibit increasing failure rates over time, baked PCBs generally demonstrate a longer operational life before failure compared to moist PCBs.

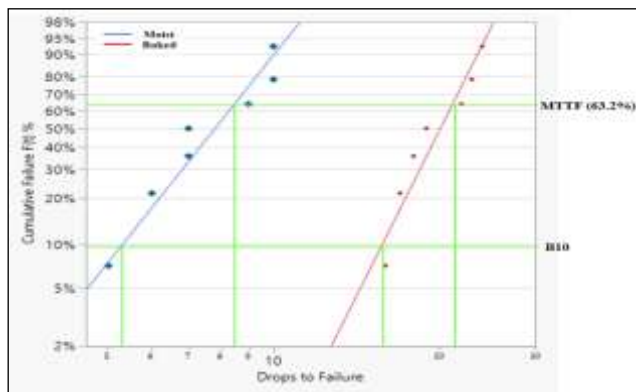


Fig. 17 Weibull distribution of the drops to failure for Moist and Baked PCBA Samples

Table 5. Analysis of the Weibull distribution plot for Moist and Baked PCBA's

Condition of PCBA	(N) Number of Samples	Shape Parameter(β)	Scale parameter(η)
Moist	7	4.86	8.44
Baked	7	7.74	21.13

6. Conclusions

This study involves preparation of Test Model by designing PCBs using KICAD software, with a single BGA mounted centrally and solder balls were daisy-chained to ensure joint

failure under drop tests. The PCBA was subjected to five service conditions of impact pulse specified by JESD22-B111, achieved by dropping the boards from different heights. Strain and impact pulse were monitored using a strain gauge rosettes and accelerometer, respectively. The drop test was simulated using the Input-G method in ABAQUS software, employing explicit dynamic analysis. The impact pulse of each service condition was used as input, and the output strain from the simulation was validated against the experimental strain.

- The strain data from each service condition was compared and overlapped with the simulated strain, demonstrating that the developed FEM model showed good correlation with the experimental results.
- Once the strains were validated, the established model was used to analyze the critical solder ball and the stresses induced in the solder balls of the BGA. The analysis revealed that the stresses in the corner most solder ball were predominant, indicating it as the vulnerable, whereas the solder ball at the center of the BGA was the least affected.
- Weibull probability plot was used to analyze the impact of moisture, indicating that moisture has a positive effect on the lifespan of solder balls under impact. Baking can improve the efficiency of the solder joints and baked PCBs generally have a longer operational life before failure compared to moist PCBs.

These findings highlight the importance of the corner solder ball's integrity in the design and reliability of PCBAs subjected to impact conditions, and the beneficial effects of baking on solder joint performance.

References

1. Jing-en Luan and Tong Yan Tee, "Novel board level drop test simulation using implicit transient analysis with input-G method," Proceedings of 6th Electronics Packaging Technology Conference, pp. 671-677, 2004. [CrossRef] [Google Scholar] [Publisher Link]
2. Fang Liu, Guang Meng, Mei Zhao and Jun feng Zhao, "Experimental and numerical analysis of BGA lead-free solder joint reliability under board-level drop impact," Microelectronics Reliability, vol. 49, no.4, pp. 79-85, 2009. [CrossRef] [Google Scholar] [Publisher Link]
3. Junfeng Zhao and L. J. Garner, "Mechanical modeling and analysis of board level drop test of electronic package," 56th Electronic Components and Technology Conference, pp.7, 2006. [CrossRef] [Google Scholar] [Publisher Link]
4. Tong Yan Tee, Jing-en Luan, E. Pek, Chwee Teck Lim and Zhaowei Zhong, "Advanced experimental and simulation techniques for analysis of dynamic responses during drop impact," 54th Electronic Components and Technology Conference, vol.1, pp.1088-1094, 2004. [CrossRef] [Google Scholar] [Publisher Link]
5. N. Muthuram and S. Saravanan, "Free fall drop impact analysis of board level electronic packages," Microelectronics Journal, vol. 129, 2022. [CrossRef] [Google Scholar] [Publisher Link]
6. Chang-Lin Yeh, Yi-Shao Lai and Chin-Li Kao, "Evaluation of board-level reliability of electronic packages under consecutive drops," Microelectronics Reliability, vol. 46. no.7, pp. 1172-1182, 2006. [CrossRef] [Google Scholar] [Publisher Link]
7. Meng-Kao Yeh and Tzu-Heng Huang, "Drop Test and Finite Element Analysis of Test Board," Procedia Engineering, vol.79, pp. 238-243, 2014. [CrossRef] [Google Scholar] [Publisher Link]

- Link]
8. Xuejun Fan, Min Pei and P. K. Bhatti, "Effect of finite element modelling techniques on solder joint fatigue life prediction of flip-chip BGA packages," 56th Electronic Components and Technology Conference, pp. 9, 2006. [CrossRef] [Google Scholar] [Publisher Link]
 9. P. Lall, S. Gupte, P. Choudhary and J. Suhling, "Solder-joint reliability in electronics under shock and vibration using explicit finite-element sub-modelling," 56th Electronic Components and Technology Conference, pp. 8, 2006. [CrossRef] [Google Scholar] [Publisher Link]
 10. Lall Pradeep, Panchagade Dhananjay, Liu Yueli, Johnson R. and Suhling Jeff, "Smeared-Property Models for Shock-Impact Reliability of Area-Array Packages," Journal of Electronic Packaging, vol.129, no.4, pp. 373–381, 2007. [CrossRef] [Google Scholar] [Publisher Link]
 11. Chung S., Kwak J.B., "Comparative Study on Reliability and Advanced Numerical Analysis of BGA Subjected to Product-Level Drop Impact Test for Portable Electronics," Electronics, vol. 9, no. 9, pp.1515, 2020. [CrossRef] [Google Scholar] [Publisher Link]
 12. Mei-Ling Wu, Jia-Shen Lan, "Reliability and failure analysis of SAC 105 and SAC 1205N lead-free solder alloys during drop test events," Microelectronics Reliability, vol. 80, pp. 213-222, 2018. [CrossRef] [Google Scholar] [Publisher Link]
 13. Darveaux Robert, Corey Reichman, Sabira Enayet, Wen-Sung Hsu and Win Thandar Swe, "Board Level Reliability Comparison of Lead-Free Alloys," SMTA International conference proceedings, 2005. [CrossRef] [Google Scholar] [Publisher Link]
 14. C. Birzer, B. Rakow, R. Steiner and J. Walter, "Drop test reliability improvement of lead-free fine pitch BGA using different solder ball composition," 27th Electronic Packaging Technology Conference, pp. 7, 2005. [CrossRef] [Google Scholar] [Publisher Link]
 15. Yuan Guozheng, Xia Chen and Xue Feng Shu, "Failure Analysis of the Solder Joints in Flip-Chip BGA Packages under Free-Drop Test," Advanced Materials Research, vol. 936, pp. 628-632, 2014. [CrossRef] [Google Scholar] [Publisher Link]
 16. C.Y. Zhou, T.X. Yu and Ricky S.W. Lee, "Drop impact tests and analysis of typical portable electronic devices," International Journal of Mechanical Sciences, vol. 50, no. 5, pp. 905-917, 2008. [CrossRef] [Google Scholar] [Publisher Link]
 17. Yuqi Wang, K.H. Low, H.L.J. Pang, K.H. Hoon, F.X. Che and Y.S. Yong, "Modeling and simulation for a drop-impact analysis of multi-layered printed circuit boards," Microelectronics Reliability, vol. 46, no. 2-4, pp. 558-573, 2006. [CrossRef] [Google Scholar] [Publisher Link]
 18. Wang. Y, "Drop impact analysis of packaged electronic products containing nonlinear cushion buffers and multilayer circuit boards," Doctoral Thesis, Nanyang Technological University, Singapore, 2008. [CrossRef] [Google Scholar] [Publisher Link]
 19. Xin Qu, Zhaoyi Chen, Bo Qi, Taekoo Lee and Jiaji Wang, "Board level drop test and simulation of leaded and lead-free BGA-PCB Assembly," Microelectronics Reliability, vol.47, pp. 2197-2204, 2007. [CrossRef] [Google Scholar] [Publisher Link]
 20. Lou Haohuan, Qu Xin, Chen Zhaoyi, Wang Jiaji, Taekoo Lee and Hui Wang, "Lifetime Assessment of Solder Joints of BGA Package in Board Level Drop Test," 6th International Conference on Electronic Packaging Technology, pp. 1-5, 2005. [CrossRef] [Google Scholar] [Publisher Link]
 21. Shao. J, Zhang H., Chen B., "Experimental Study on the Reliability of PBGA Electronic Packaging under Shock Loading," Electronics, vol. 8, no.3, pp. 279, 2019. [CrossRef] [Google Scholar] [Publisher Link]
 22. E. H. Wong, Y-W Mai and S. K. W. Seah, "Board Level Drop Impact Fundamental and Parametric Analysis," Journal of Electronic Packaging, vol. 127, no. 4, pp. 496-502, 2005. [CrossRef] [Google Scholar] [Publisher Link]
 23. E. S. Ibe, K. I. Loh, Jing-en Luan and Tong Yan Tee, "Effect of unfilled underfills on drop impact reliability performance of area array packages," 56th Electronic Components and

- Technology Conference, pp. 5, 2006. [CrossRef] [Google Scholar] [Publisher Link]
24. X. Fan and A. S. Ranouta, "Finite Element Modelling of System Design and Testing Conditions for Component Solder Ball Reliability Under Impact," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 2, no. 11, pp. 1802-1810, 2012. [CrossRef] [Google Scholar] [Publisher Link]
25. S. Chang, E. S. Ibe, K. I. Loh and K. Lamb, "Effect of underfills on board level reliability of area array package with stress calculation," *5th International Microsystems Packaging Assembly and Circuits Technology Conference*, pp. 1-4, 2010. [CrossRef] [Google Scholar] [Publisher Link]
26. D. Cadge, J. Wang H.J., R. Bai and P. Gong, "Drop Test Simulation of Electronic Devices using Finite Element Method," *International Conference on Electronic Materials and Packaging*, pp. 1-7, 2006. [CrossRef] [Google Scholar] [Publisher Link]
27. Tempelman, E., Dwaikat, M.M.S, and Spitás, C, "Experimental and Analytical Study of Free-Fall Drop Impact Testing of Portable Products," *Experimental Mechanics*, vol. 52, pp. 1385–1395, 2012. [CrossRef] [Google Scholar] [Publisher Link]
28. Zain Mohamed, Ani Fakhrozi, Ramli Mohamad, Jalar Azman & Abu Bakar Maria, Effect of Moisture Content on Crack Formation During Reflow Soldering of Ball Grid Array (BGA) Component, *Advances in Robotics, Automation and Data Analytics: Springer Nature*, vol. 1350, pp. 309-314, 2021. [CrossRef] [Google Scholar] [Publisher Link]
29. Qiu Baojun, Xiong Jingang, Wang Han, Zhou Shuai, Yang Xiuding, Lin Zhengpei, Liu Maolin and Cai Nian, "Survey on Fatigue Life Prediction of BGA Solder Joint," *Electronics*, vol. 11, no. 4, pp. 542, 2022. [CrossRef] [Google Scholar] [Publisher Link]
30. Fan Xuejun, Zhang, G.Q., Driel Willem and Ernst, L.J., "Interfacial Delamination Mechanisms During Soldering Reflow with Moisture Preconditioning," *IEEE Transactions on Components and Packaging Technologies*, vol. 31, no. 2, pp. 252-259, 2008. [CrossRef] [Google Scholar] [Publisher Link]
31. Ambosta, Samuel Terrence. "Study of the effect of humidity on thermal cycling of a ball grid array (BGA) package," M.S. Thesis, The University of Texas at Arlington, USA, 2018. [CrossRef] [Google Scholar] [Publisher Link]
32. Ferguson, Timothy P, "Moisture and interfacial adhesion in microelectronic assemblies," Doctoral Thesis, Georgia Institute of Technology, USA, 2004. [CrossRef] [Google Scholar] [Publisher Link]
33. JEDEC Standard JESD22-B111, Board Level Drop Test Method of Components for Handheld Electronic Products, JEDEC Solid State Technology Assoc., 2003. [CrossRef] [Google Scholar] [Publisher Link]
34. Abaqus user Manual (version 6.5), ABAQUS, Inc. 2005. [CrossRef] [Google Scholar] [Publisher Link]