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Development Of Interactive Web-Based Framework For Comprehensive I-V And Analog Characterization Of Nanoscale Ringfet Devices Using Python And Django

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In this work a online computational tool is developed to enhance the growth of nano-technology. This platform employs the fundamental mathematical equations to govern the physics of the FET devices. Here Python 3.6 programming IDLE has been employed to develop the web platform of the analytical model of Bulk-MOSFET, RingFET, DG-RingFET and TFET. On this platform a user can investigate the basic electrostatic characteristics of the device such as Surface Potential, Drain Current, Transconductance, Threshold Voltage, Electric Field. Also,Having the functionality of comparing the desired characteristic of one device with another device. The influence of Vds on surface potential ,drain radius on RingFET has also been demonstrated using the online tool. To make sure the result obtained from computational tool is also been verified with the result obtained from software(Such as ATLAS).

1. INTRODUCTION

The **field-effect transistor** (**FET**) is an electronic device which uses an electric field to control the flow of current. FETs are 3-terminalled devices, having a source, gate, and drain terminal. FETs control the flow of current by the application of a voltage to the gate terminal, which in turn alters the conductivity between the drain and source terminals the transistor is approaching its limits of scaling. The steady downscaling of transistor dimensions over the past two decades has been the main motivation to the growth of silicon integrated circuits. Channel lengths of 0.25 μm down to 45nm are now the norm. The more an IC is scaled, the higher becomes its packing density, the higher its circuit speed, the lower its power dissipation. However, reducing the source-to-drain spacing (channel length) of a MOSFET has led to undesirable short channel effects. The most undesirable short-channel effect is the reduction in the gate threshold voltage at which device turns on To achieve the desired goals advance Innovative device architectures, such as double-gate MOSFETs, silicon on insulator

MOSFETs, gate-all-around MOSFETs, FinFET's, and tunnel FETs ,are now given extensive consideration. These architectures possess enhanced electrostatic gate Controllability along with the superior short channel immunity The suitability of Ring-FET for sensing applicationsFig. 1.1(a)-(c) shows different orientation views of a bulk MOSFET and a RingFET architecture to illustrate the difference in the device architectures **[1]**. It can be seen from Fig .1(a) that the RingFET can be obtained by rotating the bulk MOSFET along the vertical direction. In the RingFET architecture, the gate is actively present only over the channel as in the case of the bulk MOSFET, and the gate is in a circular form. In addition, the active S/D area is asymmetric in the RingFET depending upon whether the drain is present inside the channel or outside. Thus, the RingFET architecture also comes into the category of single-gate devices, i.e. single gate bulk MOSFET, having circular geometry as depicted in Fig 1(b).

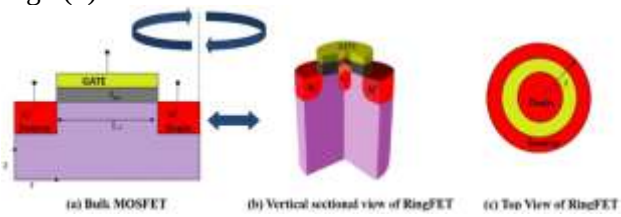

Fig.1.1(a)-(c): Bulk MOSFET, Vertical cross-section of RingFET, Top view of RingFET

Although a lot of simulation studies have already been performed, an analytical model for the RingFET architecture at a nanoscale regime has not yet been developed. Thus , to better understand the mechanism of device operation, it is very important to develop a physics-based analytical model for the same. Therefore, a physics-based 2-D analytical model for the RingFET architecture has been developed. After deriving surface potential, the model has been extended up to the drain current model. In addition, the electric field, the threshold voltage, the sub-threshold slope (SS), and the drain induced barrier lowering (DIBL have also been calculated using the developed analytical model. The RingFET architecture, as shown in Fig. 1.1(b), has been simulated using an Python and compare it with result obtain from ATLAS 3D device simulator .

There are two types of scaling are common:

1) constant field scaling

2) constant voltage scaling.

1.1 SHORT CHANNEL EFFECTS

Short-channel effects occur when the channel length is the same order of magnitude as the depletion-layer widths of the source and drain junction[3]. In MOSFETs, channel lengths must be greater than the sum of the drain and source depletion widths to avoid edge effects. Otherwise, a number of effects appear. The major issues encountered in scaling bulk MOSFET are given as:

- Drain Induced Barrier Lowering (DIBL)
- Punch-Through
- Hot Carrier Effects

2. MODELLING

2.1 Electric Field Modeling

Electric field of the device is given as the rate of change of surface potential per unit length of the channel .

$$E(r,z) = \frac{-d\Psi(r,z)}{dr}$$

2.2 Drain Current Modeling

To derive the expression for drain current of the device a threshold based model (which is based on regional approach) has been used. First of all the sub-threshold current of the device has been evaluated by integrating the channel potential over complete channel region as given below.

$$I_d = \begin{cases} I_{d_{sub}} \text{ for } V_{gs} \leq V_{th} \text{and } V_{ds} \leq V_{dsat} \\ I_{d_{lin}} \text{ for } V_{gs} \geq V_{th} \text{ and } V_{ds} \leq V_{dsat} \\ I_{d_{sat}} \text{for } V_{gs} \geq V_{th} \text{ and } V_{ds} \geq V_{dsat} \end{cases}$$

3. RESULT AND DISCUSSION

3.1 Graph between Surface potential vs. position of channel.

In fig.3(a), shows the graph between Surface potential vs. Position along the channel. Here, On the GUI user can input the values of variables(Vgs & Vds) by default they are set to 0.By clicking on the compute button user can get the output of below result Also, the user can compare the surface potential of ringFET with other devices(such as DG_RingFET,Bulk MOSFET) by simply click on the button seen below the graph.

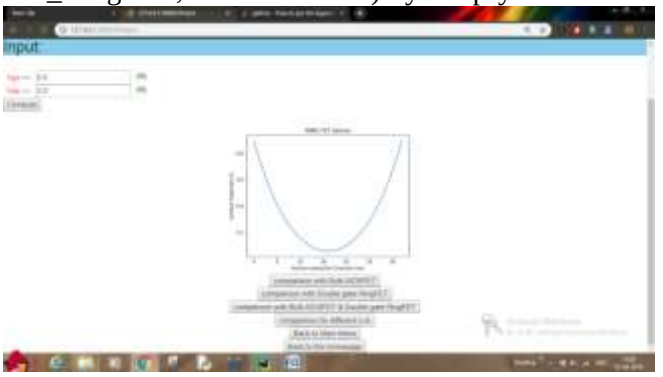

Fig. 3(a). screenshot of graph between surface potential vs. channel length at Vds = 0V.

3.2 Comparison of plot between surface potential vs. Position along the channel of bulk MOSFET and RingFET.

In fig.3(b), shows the graph between Surface potential vs. Position along the channel of Bulk MOSFET and RingFET . Here, On the GUI window user can input the values of

variables(Vgs & Vds) by default they are set to 0. Also, the user can compare the surface potential of ringFET with other devices(such as DG_RingFET,Bulk MOSFET) by simply click on the button seen below the graph.

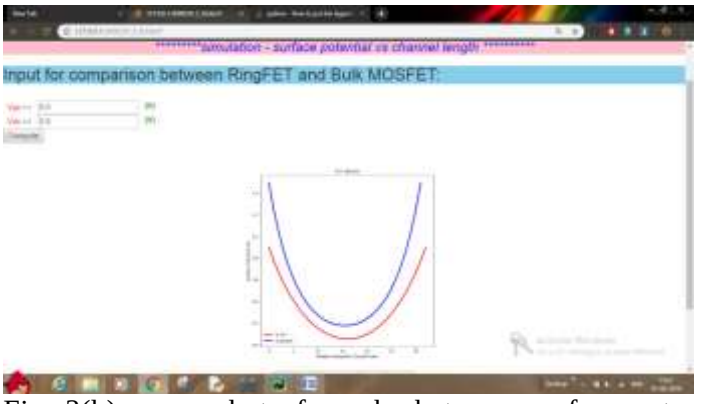

Fig. 3(b). screenshot of graph between surface potential vs. channel length of Bulk MOSFET and RingFET.

3.3 Comparison of Graph between surface potential vs. Position along the channel of RingFET and Double Gate RingFET.

In fig.3(c), shows the graph between Surface potential vs. Position along the channel of DG_RingFET and RingFET . Here, On the GUI window user can input the values of variables(Vgs & Vds) by default they are set to 0.

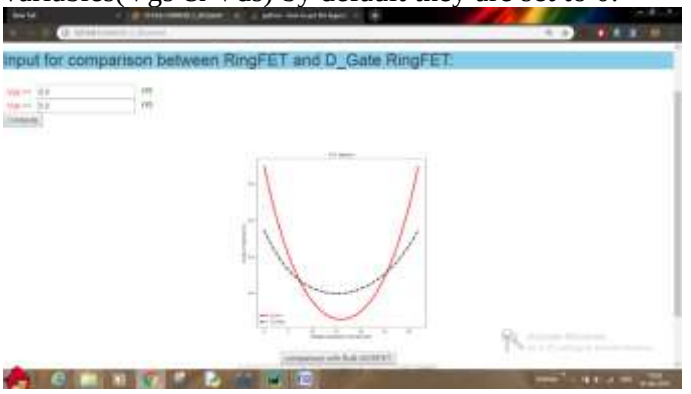

Fig. 3(c). screenshot of graph between surface potential vs. channel length of DG_RingFET and RingFET.

3.4 Comparison of Graph between surface potential vs. Position along the channel of RingFET and DG_RingFET.

In fig.3(d), shows the graph between Surface potential vs. Position along the channel of DG_RingFET and RingFET at Vds changes to 0.5V.

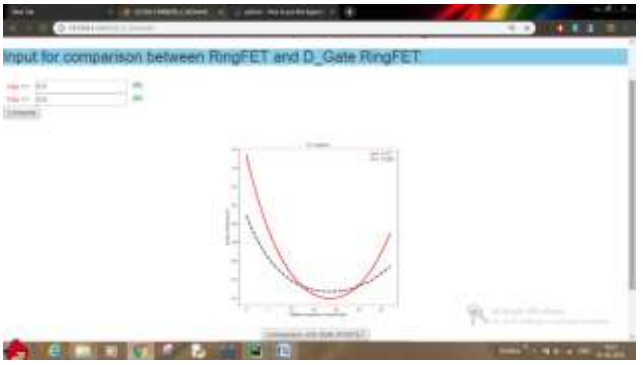

Fig. 3(d). screenshot of graph between surface potential vs. channel length of DG_RingFET and RingFET at Vds = 0.5V.

3.5 Comparison of Graph between surface potential vs. Position along the channel of RingFET , DG_RingFET and Bulk MOSFET.
In fig.3(e), shows the graph between Surface potential vs. Position along the channel of DG_RingFET ,RingFET and Bulk MOSFET . Here, On the GUI user can input the values of variables(Vgs & Vds) by default they are set to 0.

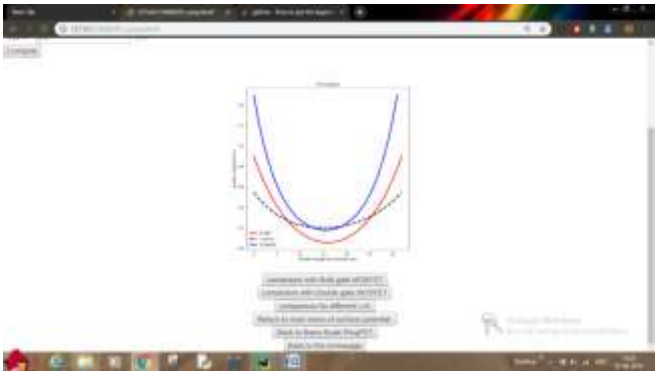

Fig. 3(e). screenshot of graph between surface potential vs. channel length of DG_RingFET,RingFET and Bulk MOSFET.

3.6 Comparison of Graph between surface potential vs. Position along the channel of RingFET for different values of Lch.
In fig.3(f), shows the graph between Surface potential vs. Position along the channel for different channel length at Vds = 0V.

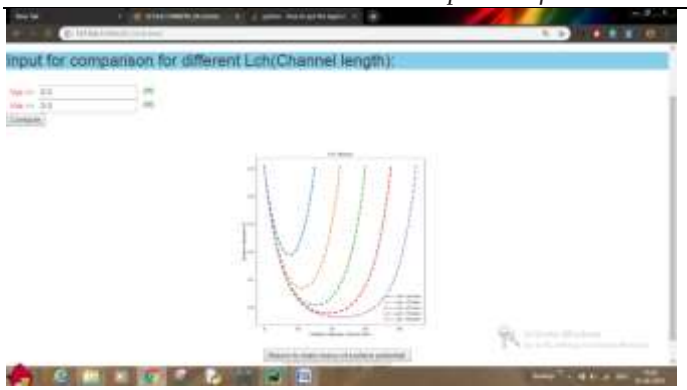

Fig. 3(f). screenshot of graph between surface potential vs. channel length of RingFET for different values of channel length(Lch).

3.7 Graph between Drain Current vs. Gate Bias(V).

In fig.3(g), shows the graph between Drain Current vs. Gate Bias(V).By clicking on the compute button user can get the output of below result Also, the user can compare the Drain Current of ringFET with other devices(such as DG_RingFET,Bulk MOSFET) by simply click on the buttons seen below the graph.

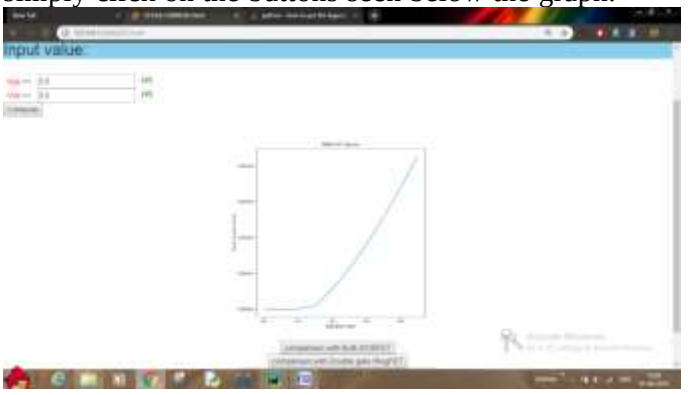

Fig. 3(g). screenshot of graph between Drain Current vs. Gate Bias(V).

3.8 Graph between Drain Current vs. Gate Bias(V).

In fig.3(h), shows the graph of comparison between Drain Current vs. Gate Bias(V) of Bulk MOSFET and RingFET.By clicking on the compute button user can get the output of below result Also, the user can compare the Drain Current of ringFET with other devices(such as DG_RingFET) by simply click on the buttons seen below the graph.

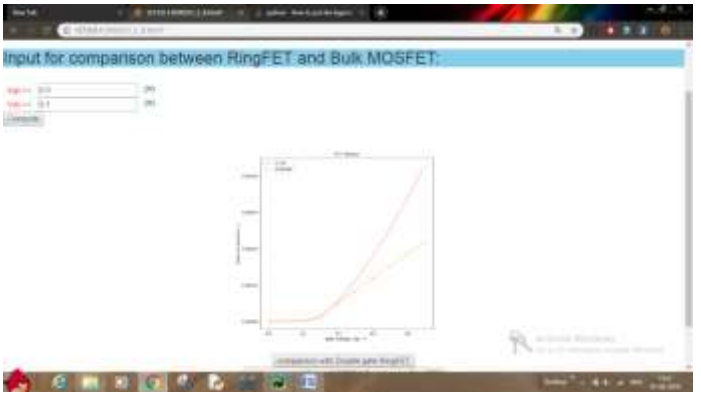

Fig. 3(h). screenshot of graph between Drain Current vs. Gate Bias(V).

3.9 Graph between Drain Current vs. Gate Bias(V).
In fig.3(i), shows the graph of comparison between Drain Current vs. Gate Bias(V) of DG_RingFET and RingFET.By clicking on the compute button user can get the output of below result Also, the user can compare the Drain Current of ringFET with other devicesby simply click on the buttons seen below the graph.

Fig. 3(i). screenshot of graph between Drain Current vs. Gate Bias(V).

3.10 Graph between Drain Current vs. Gate Bias(V).
In fig.3(j), shows the graph of comparison between Drain Current vs. Gate Bias(V) of DG_RingFET and RingFET and Bulk MOSFET .By clicking on the compute button user can get the output of below result.

Fig. 3(j). screenshot of graph between Drain Current vs. Gate Bias(V).

3.11 Graph between Threshold Voltgage(V) vs. Gate length(nm).
In fig.5.1(k), shows the graph of comparison between Threshold Voltgage(V) vs. Gate length(nm) of RingFET.By clicking on the compute button user can get the output of below result.

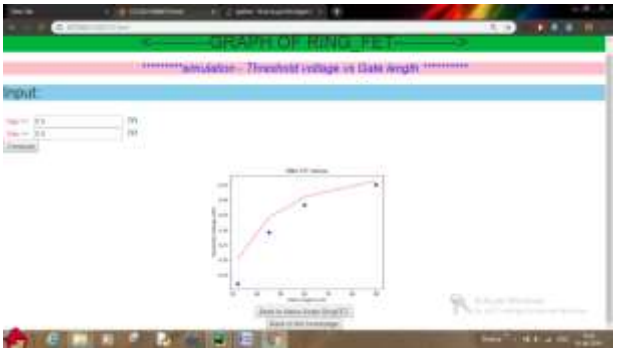

Fig. 3(k). screenshot of graph between Threshold Voltgage(V) vs. Gate length(nm)

5.1.12 Graph between Transconductance vs. Gate Bias(V)
In fig.5.1(l), shows the graph of comparison between Transconductance vs. Gate Bias(V)of RingFET.By clicking on the compute button user can get the output of below result.

Fig. 3(l). screenshot of graph between Transconductance vs. Gate Bias(V)

3.13 Graph between sub-threshold slope vs. Gate length.

In fig.5.1(m), shows the graph of comparison between sub-threshold slope vs. Gate length.of RingFET.By clicking on the compute button user can get the output of below result.

Fig. 3(l). screenshot of graph between sub-threshold vs. Gate length.

Also the workflow of the module can be understood from the flowchart given below.

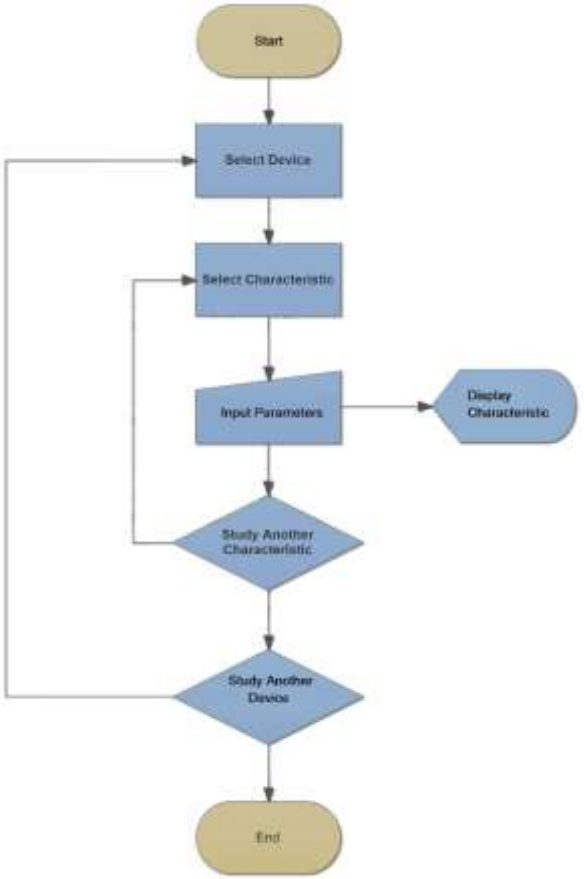

Fig.2. Flow Chart showing workflow of the computational module.

4. CONCLUSION

In this project, a web based computational module has been deployed, which is capable of studying the characteristic of FET devices like Bulk MOSFET, RingFET, DG-RingFET and TFET. The developed module is also capable of comparing the characteristics of listed devices. Also, a brief idea about the modeling and simulation of FET devices has been discussed during the project, The analytical model has been developed by solving poisson's 2-D equation for calculating the charge inside the channel region, which has been further extended to calculate other device performance matrices. . In this project simulated results have been obtained from ATLAS device simulator.The developed platform facilitates the user with a handy functionality to study device characteristics. Web interface of the module has been developed by using FLASK which at the back end uses PYTHON as high level programming language to solve complex system of mathematical equations. To make it possible on a single platform **PyCharm** (primarily developed by jetbrains) is used as IDLE (Integrated Development and Learning Environment)[4]. In pycharm anumber of modules has been used to develop the model forRingFET and other devices listed in the computational module,. Some of the modules used in this project areNumpy, Sympy, Matplotlib, Scipy, Jinja2 have played a key role in developing the complex model for the above mentioned devices. . In this project to writing the equations in the form of code was a bit complicated task.In addition to it having an interaction among different modules was also a challenging task.Also, having the knowledge of modules to be used is a pre-requisite: why??

Because each module hasits unique workspace with uniquely defined capabilities.Thatmeansone should haveknowledge of which module shall be used for a particular process.

In this project, it is first ever when we compare the two device characteristics simultaneously on web access either on Mobile-phone or on PC. During this project, bug on each and every stage in code giving a advantage of learning something new in the python. Moreover, to connect one module to another module is a great challenge in this project. Say, the interaction of Nympy with Sympy was one of the challenging task in this project but after dealingwith a numberof bugs/error we did it and rescuedour code from every problem came during this project, either it is ofusingScipy while solving first/second kind of Bessel functions or of solving complex calculations of modeling parameters using mathematical modules.The main goal of this project was to develop an open access web based characterization platform to make the simulation reliable and feasible for entire student fraternity was achieved to some extent. Also there is a lot left to explore and do in this project.

5. FUTURE SCOPE

As online simulators serves more than 2 million users yearly [9].computational scientists, experimentalists, educators, and students get benefit from these online simulation tools.

This platform can beused to hosta rapidly growing collection of simulation tools for Nanoscale phenomena that run in the cloud and are accessible through a web browser. In addition to

simulations, this provides online comparison between the different devices and also we can download the results too, animations and more. These resources help users to learn about our simulation tools and about Nanotechnology in general. A good starting page for those new to our application or to Nanotechnology is the education page. Also, we will offers researchers a venue to explore, collaborate, and publish content, as well. Much of these collaborative efforts occur via workspaces, user groups, and projects and adds powerful analytical and predictive capabilities for researchers.

This work will impacts industry, education, and governmental organizations around the world, Basically most of the user are from industry, institution and also from the government organization so this kind of tool will help them.

This platform can be further extended to incorporate all latest proposed devices with their modeling and simulation data. Also the platform can availed with facility of ease of access so that each willing user may add their own developed modules.

So go ahead! Start developing the online tool with great features. Of course, user can simulate anytime and anywhere having no restriction of undesirable factors i.e by the time mobile phone is used as a simulator tool for Nano-technology evolution. This will save time and speed up the contribution of researchers/scientist. So, in the era of clouding this will enhance the reliability and add quality to the work of users.

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