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Design Of A Phase-Locked Loop Using Current Starved Voltage Controlled Ring Oscillator In 45nm Technology

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This paper discovers a PLL core design that can achieve wide range of frequency. As we know that the main block of PLL is voltage control oscillator (VCO). For achievement of high oscillation frequency, good stability, a ring oscillator that uses current starving technique has been designed. Based on the circuit the PLL is designed using Cadence tool in 45 nm technology.

Keywords—Phase Locked Loop[PLL],Current Starved Voltage Controlled Ring Oscillator (CSVCRO), Phase detector, D-Flip Flop, Charge pump with LPF, Frequency divider, High frequency.

I. INTRODUCTION

Designing a Phase-Locked Loop (PLL) with a high-frequency VCRO(Voltage Controlled Ring Oscillator) in 45nm technology requires achieving of precise frequency synthesis and noise suppression. PLLs are essential in various applications such as clock generation, frequency synthesis and bio-medical applications where stability, low noise and accuracy are important.

The VCRO used in PLL design offers several advantages, including low phase noise characteristics and high-frequency operation which are crucial for modern high-speed communication systems and RF applications.

The 45nm technology node is an advanced semiconductor process node which offers improved performance and integration capabilities, making it the primary choice for implementing complex analog and mixed-signal circuits like PLLs.

Careful attention must be paid to biasing schemes, device sizing, circuit topologies, and layout techniques to enhance performance metrics namely locking range, phase noise, area efficiency, and consumption of power in the design. Advanced CAD tools and simulation methodologies play an important role in the design and verification process, which enable accurate performance prediction and design optimization before fabrication.

To implement PLL circuit successfully, one requires a deep understanding of analog and circuit design principles, knowledge in semiconductor device physics and fabrication technologies.
Thus, designing a PLL using a high frequency VCRO in 45 nm technology will need the combination of both theoretical and practical expertise to meet the demands of modern high-speed communication systems.

A PLL can be explained as a feedback control system which produces a resultant signal where the phase is controlled by the phase of an input stimuli.

The primary objective of PLL circuit will synchronize the phases of generated output signal and input signal.

PLLs are widely used in various applications, including phase modulation, clock recovery, frequency synthesis, demodulation, and among others.

This circuit comprises of the given elements:- phase detector, a LPF, VCO and involves a series of steps for its operation.[1]

The PLL designed using a high-frequency Voltage Controlled Ring Oscillator (VCRO) in 45nm technology represents a remarkable advancement in the field of analog and RF circuit design. PLLs are predominant in modern electronic systems, used for frequency synthesis, clock generation, and phase alignment. The integration of a VCRO provides an excellent performance in terms of frequency and phase noise characteristics, making it a notable option for high-speed RF applications and communication systems .

Overall, the design of a PLL using a high-frequency VCRO in 45nm technology depicts a phenomenal progress in analog and RF circuit design.

Through careful optimization of device parameters, circuit topologies, and layout techniques, we can achieve outstanding performance characteristics, that are critical to meet the rising requirements of modern electronic devices and communication systems.

The Phase detector will compare both division signal(feedback signal) and reference signal and generate an output which will be in proportion to the phase difference amongst the two input frequencies. The charge pump and anti-aliasing filter are involved to considerably enhance the PLL capture range [2].

The rest of the paper is segregated in given format: section II explains the conventional PLL, section III explains about the proposed circuit design implementation of PLL, section IV explains about the simulation results and comparisons respectively, section V concludes the paper followed with the list of references used.

II. CONVENTIONAL PHASE LOCKED LOOP

PLLs helps in calculating system disturbances in the devices that monitor power quality and also included in GPS systems. They provide synchronized clock pulses to microprocessors, memory modules etc.

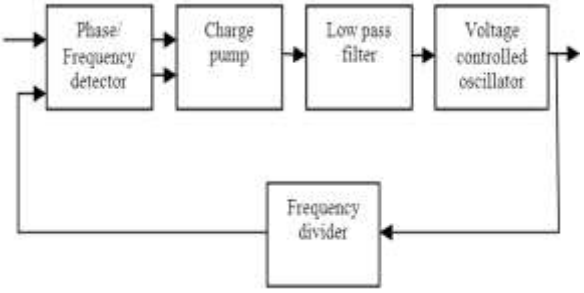

Fig.1: Simple Block diagram of a PLL

i)Phase Detector

Phase Detector is the element that compares the applied inputs and will produce an error signal as output which is in proportion with the phase difference between the frequencies of applied input signals. These circuits are implemented in applications like radar, servo-mechanical systems and demodulators.[5]

ii) Charge pump with low pass filter

A charge pump circuit will take in the DC voltage as input and generates an output current in proportion to the DC voltage to charge the capacitors present in it.

iii)LPF or Low Pass Filter

The LPF will block the higher range frequency pulses of the applied input and generates a DC voltage to drive the VCRO.

iv) Voltage Controlled Ring Oscillator [VCRO]

A CMOS VCRO is designed using multiple number of inverters in odd combinations in the form of a ring, the prior stage resultant wave is given as feedback to the input of the current stage such that every inverter will have an identical propagation delay (Δt). To obtain sustained oscillations without any distortion, the ring oscillator should meet the Barkhausen criteria:

(1) The overall phase shift of a signal all around the loop travelling through an amplifier and a feedback network is 360 degrees or 0 degree.

(2) Given open loop gain (A) and feedback factor (β),the magnitude of the product of them should be unity. (i.e.) $|A\beta|=1$.

Figure 2 shows us the schematic representation of the ring oscillator with N-stages and the figure 3 depicts the 3-staged conventional ring Oscillator. Every delay stage is a combination of NMOS and PMOS transistors.[8]

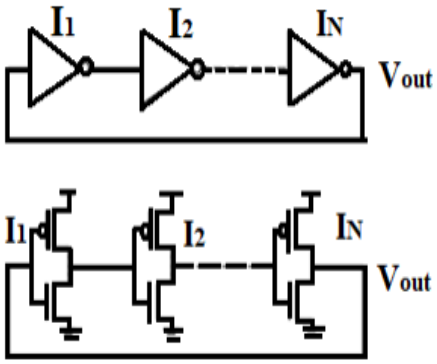

Fig. 2: CMOS based Ring Oscillator

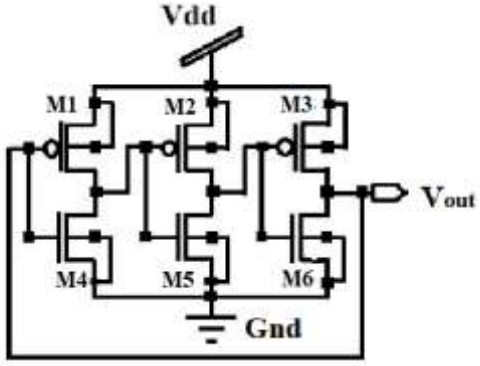

Fig.3: Three stage delay CMOS ring oscillator

v)Frequency divider

The frequency divider circuit will divide the applied signal's frequency by a factor of "n" where n is either an integer or a fraction.

III.PROPOSED CIRCUIT IMPLEMENTATION

The PLL is an important component in many daily life applications and are widely used in many control systems, multimedia applications etc.

The proposed Phase Locked Loop design comprises of the components which are used in conventional PLL but to get good results of PLL, we have proposed Current Starved Voltage Controlled Ring Oscillator[CSVCRO] in this paper.

i)Phase Detector (PD)

This is designed using D-FFs and one Nand gate. It will compare the given two inputs: reference signal, VCO signal whose frequency is reduced by a factor of "n"[division signal] by frequency divider at every pulse and will generate two signals named as 'UP' and 'DOWN' based on the phase difference that is present between the frequencies and start time of their edges.

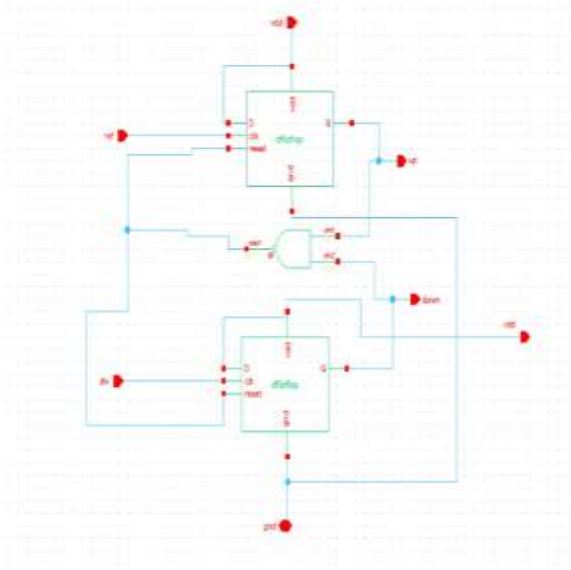

Fig.4: Schematic design of the Phase Detector

When the reference pulse leads the CSVCO, the UP signal goes high and will remain until the CSVCO pulse goes high. This indicates that the VCO frequency should be increased. When the CSVCO pulse leads the reference pulse; the DOWN signal becomes 1 and will remain until the reference pulse goes high. This indicates that the CSVCO frequency should be decreased.[6]

ii) Charge Pump with LPF

The charge pump implementation deals with low pass filter which comprise of one Pull-Up network & one Pull-Down network. The operation of this diagram is explained as below:

(1) When the UP signal is 1v, P0 transistor will be 0^{th} state, and the I0 current source will drive P2. Thus,P2 will turn ON, but the voltage headroom present in the middle of source and gate of transistor P1 isn't adequate to open it. Similar to P2 transistor,P4 will also enters into 'ON' state and now P2 and P4 will act as a current mirror. The Current Source I0 will charge the Capacitor Cp, increasing the voltage V_c. Whereas DN signal is in Low logical level, thus the whole Pull-Down network will be open circuit. When the UP signal becomes zero(Logic Low), the transistors P0,P1 will 'ON'. Since I0+IP1=IP0, transistors P2,P4 currents are very low hence they become unimportant. The capacitor voltage V_c has to remain unchanged. P3 and N0 helps to predischarge the P4 gate.If they are not used in this pump circuit, when the UP signal is transitioned from low to high, the charging time of P2 becomes more, which results in postponing time to open P4. ∴ To overcome this issue, N0 and P3 are used at the gate of P4. They both helps in pulling down the gate of P4 faster to open the P4 transistor.

(2)On the other hand, when DN goes high, Pull-Down network will become 'ON' and the discharge of capacitor Cp happens. When both UP and DOWN turns ON, the circuit operate in the saturation region. Thus, to maintain the identical current levels, N0 and P3 should be perfectly matched (IP3=IN0).

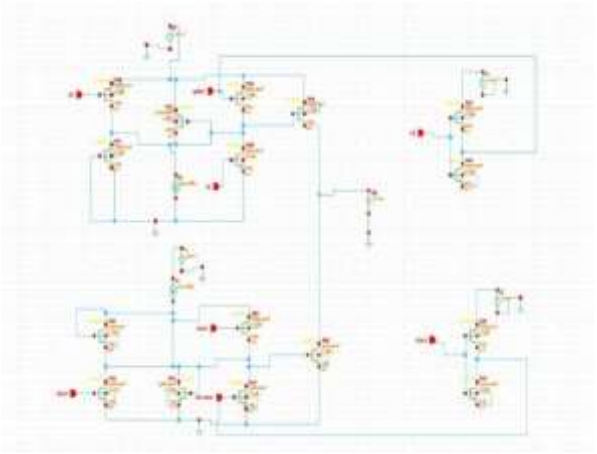

Fig. 5: Schematic of charge pump with low pass filter

This signal will be sent to a low-pass filter for high frequency components elimination. It will produce a DC voltage named as "V_{ctrl}" to feed it to VCO.

iii) Current Starved Voltage Controlled Ring Oscillator

The VCO used in the design is Current Starved Voltage Controlled Ring Oscillator[CSVCRO].The CSVCRO is one in which the delay of the inverter stages is regulated by restricting the amount of current which is used to discharge or charge the inverter stages' capacitive loads.

By varying the control voltage [V_{Ctrl}], we can vary the frequency ranges of the oscillator.

The frequency equation of the CSVCRO is

$$f_{osc} = \frac{I_d}{2N * C_{total} * V_{Ctrl}}$$

The M5 and M8 transistors will work as not gate which are having series connection M1 and M11 will function as current source, and provide the current to the M8 and M5 transistors. The amount of current is equal for all inverter stages. Control voltage (V_{ctrl}) can be used to control the resistances of Pull-Up and Pull-Down transistor networks. By altering the adjustable resistances, the current required to charge and discharge the load capacitors can be generated. Higher the supply of control voltage, higher the current that flows, responsible of lower resistance, high frequency and minimum delay.

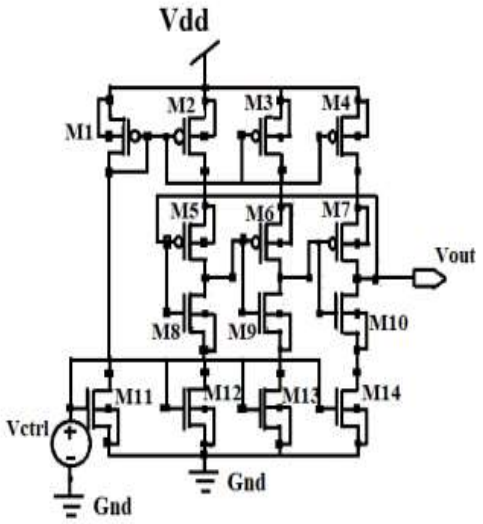

Fig :6 (a).

In general, this VCRO contains modifiable bias current to have a command over oscillator frequency. Using CSVCRO, we can achieve high frequency oscillations with low voltages.[10]

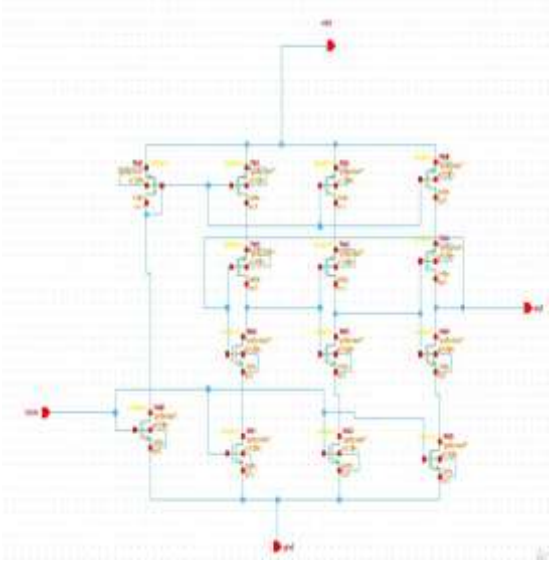

Fig:6 (b).

Fig.6(a) and 6(b): Schematics of Voltage Controlled Ring Oscillator using Current Starvation technique

iv) Frequency divider

The CSVCRO generates high frequency signals using that DC voltage. The frequency will be proportional to the DC voltage. This high frequency signal should match the frequency range of the reference signal to be compatible for the phase detector for comparison. So, a frequency divider circuit is used to part the CSVCRO frequency by a factor of "n".[9]

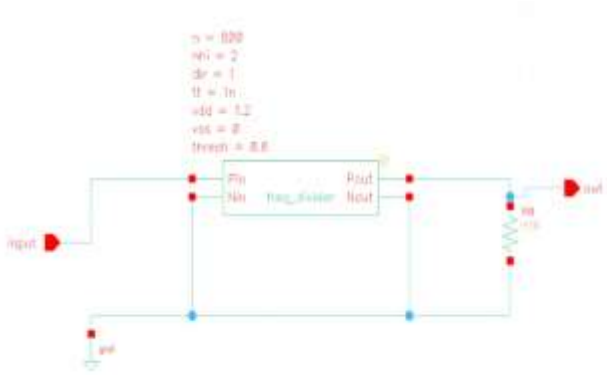

Fig. 7: Schematic diagram of Frequency divider

signal is fed to the phase detector for repeating the process. Whenever the phase difference between the signals changes, the output of phase detector changes and a new respective error voltage is generated for VCO and the frequency is maintained stable. In this way, the VCO is adjusted to produce sustained oscillations.

When the phase difference remains constant, the Phase-Locked Loop circuit gets locked and again, when it changes, the process gets repeated.[7]

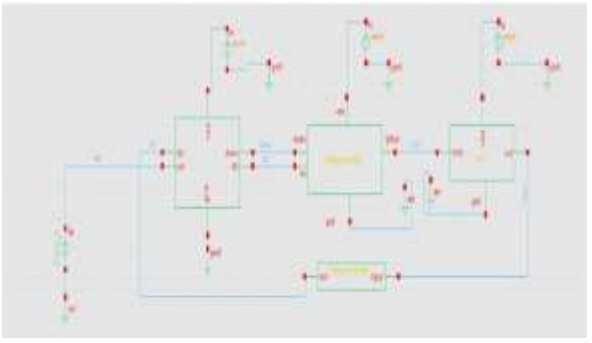

Fig.8: Schematic of phase locked loop

IV. EXPERIMENTAL RESULTS

The design and simulation of the PLL circuit is performed in the Cadence Virtuoso 45nm technology.

The simulation results are shown in the below figures:

i)Simulation output of proposed 3-stage Voltage Controlled Ring Oscillator

Fig. 9 shows the frequency of the proposed VCO. Table 1 explains the linear relation in the middle of oscillation frequency and control voltage three stage ring VCO. The V_{ctrl} is varied between range of 1-3V. The output frequency generated is ranging from 10 Giga Hertz to 39.3 Giga Hertz with some deflection.

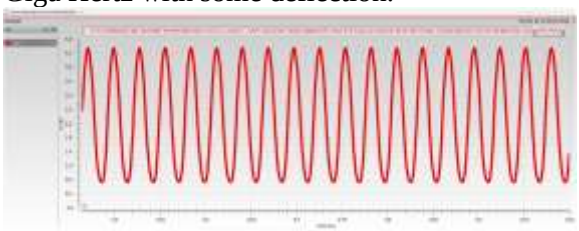

Fig.9: Output signal of proposed 3-stage ring VCO

Technology 45nm,power supply-5V	
Control voltage	Frequency of oscillations(GHz)
1V	10GHZ
2V	35.3GHZ
3V	42.4GHZ
4V	43.3GHZ
5V	43.24GHZ
4V	43.2GHZ
4V	39.3GHZ

Table.1: Simulation results of improved VCRO

ii) Simulation results of frequency divider.
The output waveform of frequency divider can be observed in Fig. 10. The Current Starved Voltage Controlled Ring Oscillator is having a high frequency of oscillation which needs to be compared with reference voltage so the oscillation frequency needs to be reduced by frequency divider, here we are dividing by 8 which gives the input as 39.3 GHz to 4.2GHz

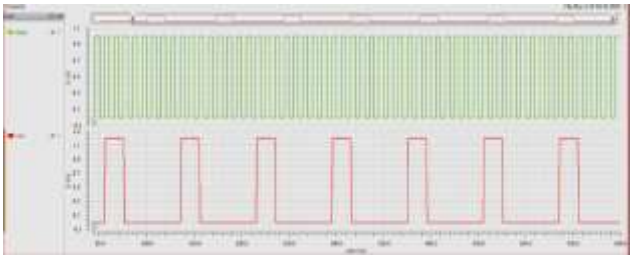

Fig.10: Output waveform of frequency divider

iii) Simulation results of the Phase Locked Loop
The PLL has been simulated and phases of the input signals are locked by output signals that can be observed from Fig. 11. The designed PLL,depicts improved functioning in terms of tuning range and lower area.

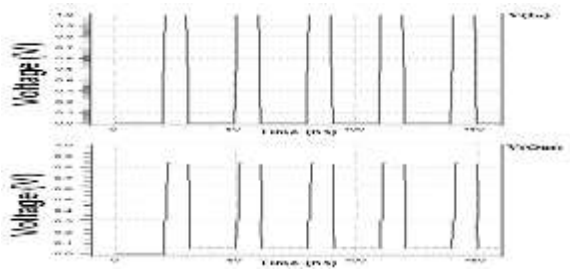

Fig.11: Output waveform of phase locked loop

V. CONCLUSION

This paper has depicted Implementation of PLL in 45nm CMOS technology using proposed high frequency CSVCRO for communication systems. The small area of PLL,and low power places it as top priority in clock generators and frequency synthesizers. The notable merits of PLL are its lock range, power consumption, size, frequency range etc.

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