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Implementation of Seed Flipping Test Pattern to Detect Faults in LBIST

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Design and manufacturing challenges posed by the increasing transistor count and shrinking feature size in modern chips have significantly heightened the occurrence of defects. As a result, rigorous testing has become indispensable in the VLSI design process. Unfortunately, amidst the lengthy design cycles, test procedures often take a back seat, overshadowed by the primary focus on design development. To ensure high quality and reliability, it is imperative that any VLSI design be entirely fault-free before deployment. Design for Testability (DFT) techniques play a crucial role in facilitating error detection and ensuring robustness during testing phases. Among these techniques, Logic Built in Self-Test (LBIST) stands out for its effectiveness in achieving comprehensive fault coverage. Here it is implemented LBIST with a focus on enhancing fault coverage for a 16-bit test pattern using SFRG (Seed Flipping Ring Generator). This approach not only maximizes fault detection capabilities but also optimizes area and power efficiency compared to alternative pattern generators. By leveraging this test pattern, we aim to address the growing complexity and reliability demands of modern integrated circuits effectively. The code is written in HDL language with Verilog code, and it is implemented using Xilinx Vivado software tool.

Keywords: Seed Flipping Ring Generator (SFRG), Built-in Self-Test (BIST), and Logic Built-in Self-Test (LBIST), Design for Testability (DFT).

1. Introduction

In recent years, the urgency and difficulty of achieving low-power designs in high-performance VLSI circuits have intensified. To address this, numerous methods have been developed to reduce power consumption in new VLSI designs, primarily focusing on optimizing power usage during functional operation rather than test mode operation. However, recent research has highlighted a critical issue: during test mode operation, switching activity can significantly increase compared to functional operation. This elevated

activity can lead to spikes in peak power dissipation, potentially causing voltage droops due to inductance, which might result in some otherwise good dies failing tests, thus reducing overall yield. Moreover, the reliability of the Circuit under Test (CUT) can be compromised by increased average power dissipation, temperature, and current density during testing. As VLSI devices grow and complexity, testing them at high levels becomes more costly. There is uncertainty whether test compression techniques will keep pace with the rapid technological advancements expected in the next decade. Interestingly, [4] Logic Built-In Self-Test (LBIST), initially designed for board, system, and in-field testing, is gaining acceptance for production testing due to its robust Design for Testability (DFT) capabilities. LBIST, often integrated with test compression techniques, represents a hybrid approach that promises enhanced test quality, faster power-aware testing, and reduced manufacturing costs while leveraging the benefits of both LBIST and scan compression. As VLSI circuit complexity continues to rise, the adoption of Built-In Self-Test (BIST) methodologies becomes increasingly essential. BIST allows the chip to test itself, evaluating circuit responses efficiently. Modern BIST methodologies often utilize pseudorandom pattern generators (PRPGs) to create test vectors. These vectors are either applied directly to the circuit or modified by additional circuitry to achieve comprehensive functional coverage.

2. Related Work

SEED FLIPPING RIGN GENERATOR

The polynomial equation $X^{16}+X^{15}+X^{13}+X^{4}+1$ defines the characteristic feedback mechanism of a 16-bit SEED (Shift register with Enable and Data input) circuit, which operates as a Linear Feedback Shift Register (LFSR)[6]. This configuration allows the SEED to generate a sequence of pseudo-random outputs based on its initial state and the specified feedback polynomial. [1] In the SEED circuit diagram shown in Fig 2.1. the feedback taps correspond to specific bit positions within the 16-bit register. These taps are crucial as they determine which bits influence the generation of subsequent bits in the sequence. In this case, the taps are located at positions 16, 15, 13, and 4, and the feedback polynomial specifies that these taps are XORed together to produce the next state of the SEED. The SEED initializes with a pre-loaded seed value, typically a non-zero value, and proceeds to generate pseudo-random outputs through successive clock cycles. The sequence length of the pseudo-random outputs is determined by the maximum period of the LFSR [2], which for a 16-bit SEED is $2^{16}-1=65535$. During operation, the SEED cycles through states based on the feedback polynomial, producing a stream of binary outputs (0s and 1s) that appear random but are deterministic based on the initial seed and polynomial configuration. This pseudo-random sequence can be utilized in various applications such as cryptography, digital signal processing, and testing. Seed flipping memory refers to modifying the initial test seeds stored in memory during testing, enhancing fault detection by exploring diverse input combinations. This seed value serves as the starting point for the pseudo-random pattern generator. Using the retrieved seed value, the pseudo-random pattern generator generates a sequence of test patterns.

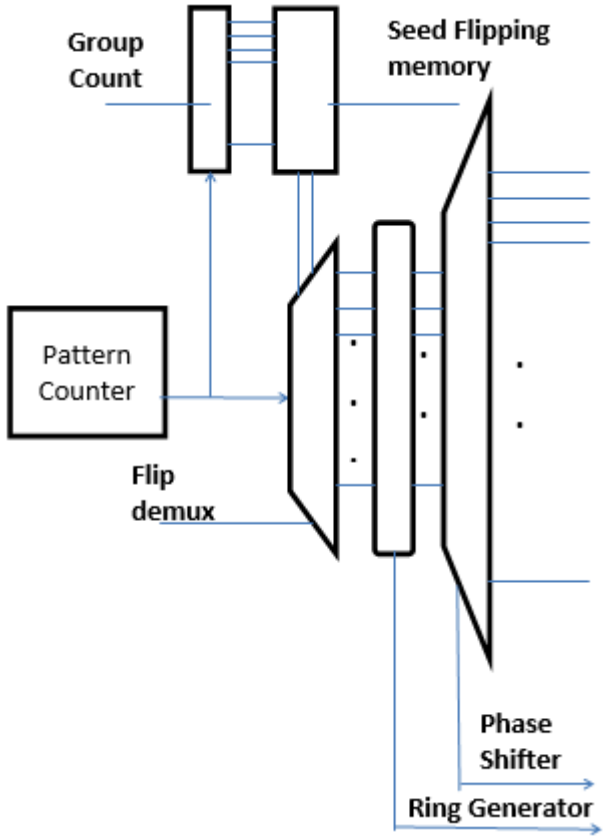

Fig.2.1. SEED FLIP RING ARCHITECTURE

Pattern counter keeps track of the number of test patterns applied, facilitating controlled variation of seeds for improved fault detection. The pattern counter is a counter register or similar mechanism used to keep track of the current pattern being generated. It increments each time a new test pattern is generated. As shown in Fig 2.2. Group counter [12] is utilized to manage and track the dynamic modification of test seeds for different sections or groups of circuits, enhancing fault coverage and test efficiency. This typically involves setting the counter to its starting value, often zero, indicating the beginning of the test pattern generation cycle.

Ring generator is employed to cyclically manipulate test seeds, ensuring systematic variation and comprehensive coverage during testing. Unlike pseudo-random pattern generators, which generate [3] Ring generator is employed to cyclically manipulate test seeds, ensuring systematic variation and comprehensive coverage during testing.

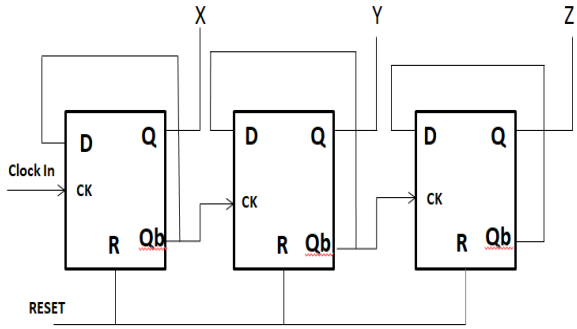

Fig.2.2. GROUP COUNTER

Unlike [10] pseudo-random pattern generators, which generate patterns randomly, the ring generator produces patterns in a deterministic manner is shown in Fig 2.3.

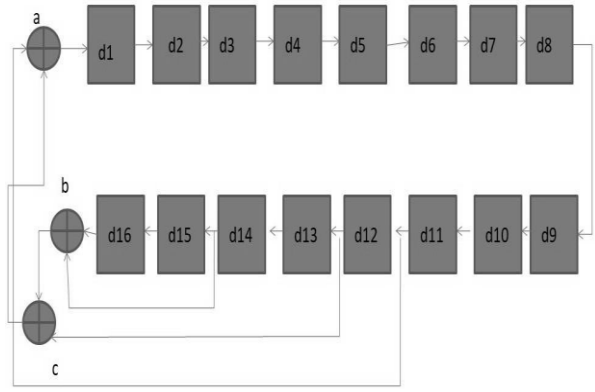

Fig. 2.3. RING GENERATOR

Phase shifter adjusts the timing relationship between test patterns, optimizing the dynamic manipulation of seeds for enhanced fault detection. The primary function of the phase shifter is to adjust the timing of test patterns [13]. This adjustment can involve delaying or advancing the timing of the test patterns relative to a reference signal, such as a clock signal. Flip de-mux acts as a control unit, selectively enabling or disabling seed manipulation for specific segments of the circuit during testing. It ensures that each part of the circuit receives a unique seed value, enabling the generation of diverse test patterns across the entire design.

3. LOGIC BUILT IN SELF TEST

Fig 3.1. Shows that LBIST Architecture that represents LBIST stands for Logic Built-In Self-Test, which is a methodology used in integrated circuit (IC) testing to ensure the functionality of digital circuits. LBIST is designed to test digital logic circuits within an IC without relying on external test equipment or access points. This makes it particularly useful

for testing complex ICs where accessing internal nodes directly for testing purposes would be impractical. [5] LBIST works by embedding special test circuitry within the design of the IC itself. This circuitry generates test patterns, applies them to the internal logic circuits, and then checks the responses to detect faults. LBIST typically uses pseudo-random or deterministic test patterns that are generated by the built-in test circuitry. These patterns are designed to comprehensively test different aspects of the digital logic, including signal paths, registers, arithmetic units, and memory elements. As the test patterns are applied, the [9] LBIST monitors the outputs of the circuit under test. It compares the actual output responses against expected responses (based on the known good design behaviour). Discrepancies indicate potential faults such as stuck-at faults, transition faults, or delay faults. [11] LBIST is primarily effective for testing digital logic circuits. It may not detect certain types of faults, such as analog circuit faults or faults that occur due to interactions between different sections of the IC[14].

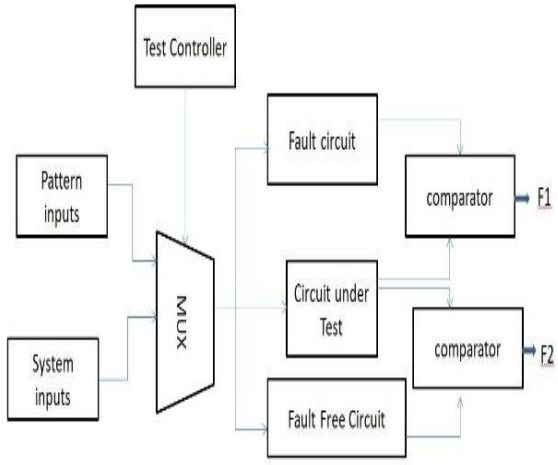

Fig.3.1. LBIST ARCHITECTURE

4. SEED FLIPPING TEST PATTERN RING GENERATOR ON LBIST

The Logic Built in Selft Test(LBIST)[7] having two inputs one is Test pattern and other primary inputs. In Testing mode, Test patterns assigned as input to LBIST. The Test pattern with 16-Bit Seed Flip Ring Generator that generated 2^n states in random generator way. A signature is taken from the DUT's outputs using a compression technique called Output Analyser. [8] The TEST controller is configured to activate the relevant blocks based on whether the LBIST is being used in testing mode or normal mode. A multiplexer (MUX) known as a 2X1 MUX is required to select between the System Inputs and the Pattern Inputs. The input to the MUX is 16 bits in size because the SEED is 16 bits in size. A vector is utilized as both the output and the input data for MUX. The choice signal of the MUX is under the control of the Test Controller. The design that will be examined is the 16-bit multiplier since, in accordance with LBIST to detect faults [15]. Comparator generates fault

and fault free with F1 and F2. F1 represents 1 it shows as the fault 0 with fault free circuit. Similarly, F2 shows 1 represents fault free 0 with circuit with fault. In advanced BIST systems, detection may be followed by attempts at self-repair, where the circuit or system attempts to correct the fault autonomously.BIST can also include real-time monitoring capabilities where the circuit continuously monitors its own performance and compares it against predefined thresholds or expected behavior. This allows for immediate detection and response to faults as they occur.

When a fault is detected, BIST systems can provide diagnostic information such as the location of the fault within the circuit or system. This information is crucial for subsequent maintenance or repair actions.

5. SIMULATION RESULTS

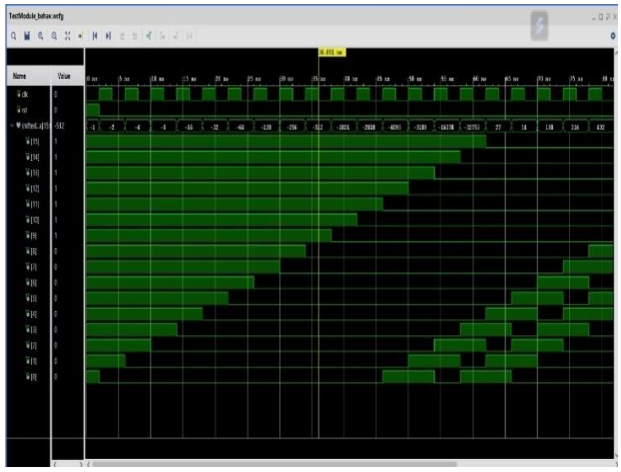

Fig 5.1. Simulation report of Seed Flip Ring Generator

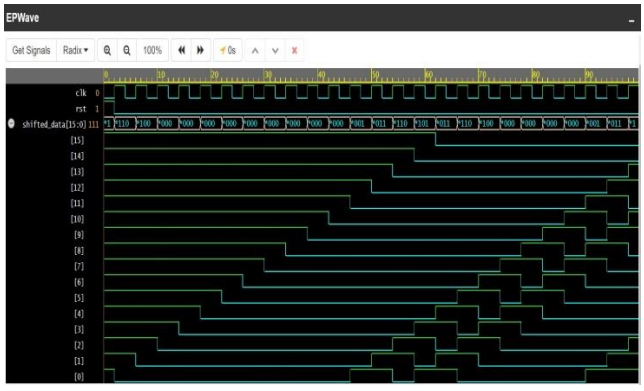

Fig 5.2. 16 Bit Seed Flip Ring Generator

Fig 5.1. & Fig 5.2. Represents the simulation report of Seed flip ring Generator, timing diagram shows that 16 bit Test pattern generated with enable high 2^{16} test patterns generated to test the any VLSI Circuits in order to detect fault in LBIST. The above test patterns will

given as input to LBIST to detect the faults.

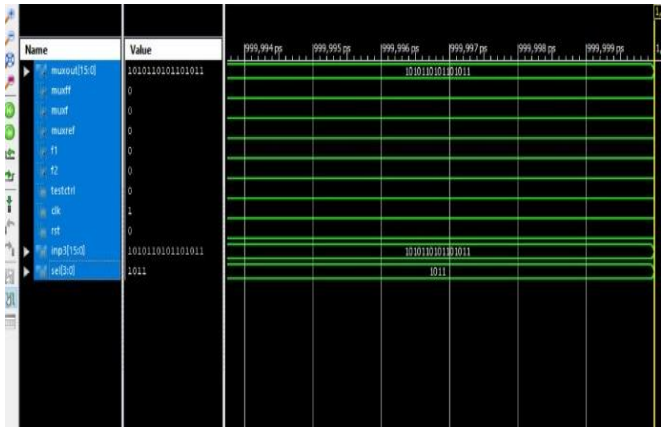

Fig 5.3. 16 Bit Test Pattern

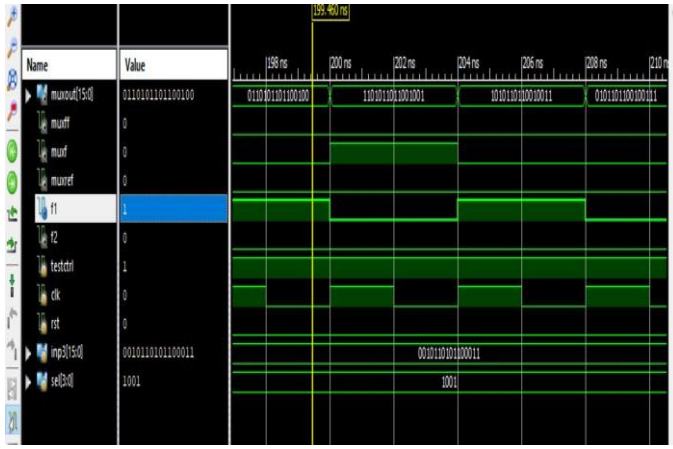

Fig.5.4. Simulation result Fault and Fault free

Fig. 5.3.& Fig.5.4 shows that detecting of faults with F1 & F2 by giving fault and fault free circuit to get output as detecting of faults.

Synthesis Report

Parameters	Low Power PRESTO with LBIST	Seed With LBIST
Total cell area	6345	1325
Total Power(uW)	34.80	18.3
Overall Compile Time (ns)	6.39	4.09

Table 1. Synthesis report of Low Power PRESTO Vs SEED applied to LBIST

6. CONCLUSION

With the rise of autonomous vehicles, ensuring the reliability and safety of automotive

systems becomes paramount. Explored a sophisticated testing method known as seed flipping. This technique involves systematically altering the initial 'seed' values used to generate random inputs or scenarios. Seed flipping enhances fault coverage by systematically varying test patterns, reducing correlation for improved fault detection. It ensures robustness, optimizing test quality and efficiency. Through this testing approach, manufacturers can enhance the fault coverage and robustness of their testing methodologies, thereby improving the overall yield, quality and reliability of their products

FUTURE SCOPE

Moreover, the implementation of seed flipping testing within LBIST frameworks underscores its significance as a versatile and efficient technique for fault detection and diagnosis, offering valuable insights into the health and performance of integrated circuits across different stages of their lifecycle, from design verification to post-silicon validation. Implemented seed flipping method to generate pseudo random sequence. This design is simulated and synthesized using Xilinx Vivado tool.

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