Design of High Speed Sense Amplifiers for SRAM IC

Km. Ankita Kumari Singh[1*] Vishal Yadav[2] Ajay Kumar Maurya[3] Ravi Prakash[4]

[1]M.Tech Students, [*]Department of Electronics Engineering*
VBS Purvanchal University, Jaunpur, U.P.
[1]Email: ankitasingh2085@gmail.com, vishalunsiet@gmail.com, ajaybtech84@gmail.com, ravirim@gmail.com*

Abstract: In today's tech-driven landscape, semiconductor chips are critical to the functionality of most modern devices, requiring compact designs and low power consumption for efficient data storage and memory. SRAM (Static Random Access Memory) is key to meeting these demands. This study leverages Cadence Virtuoso software to design a high-performance sense amplifier circuit specifically tailored for low-power SRAM applications. Various power reduction strategies were explored, resulting in an optimized solution within a redesigned SRAM architecture. The study analyzes the impact of power consumption and response time of the proposed sense amplifier by adjusting key parameters, such as the transistor width-to-length (W/L) ratio, power supply, and nanoscale technology. Detailed metrics on power usage and transistor count for different configurations are presented to identify the most effective approach. Our proposed low-power sense amplifier design shows promising results, incorporating three VLSI power reduction techniques to enhance efficiency. These innovations in low-power SRAM are poised to advance memory-centric neuromorphic computing applications.

Index Terms: Voltage Sense Amplifier, Current Sense Amplifier, Cross Coupled Sense Amplifier, Latch Sense Amplifier, hybrid mode Sense amplifier, Delay, Power-dissipation.

1. Introduction

The most critical element in VLSI chip design is SRAM-based cache memory. The performance of memory and peripheral circuitry significantly affects the overall system speed and power efficiency. In SRAM design, the delay during read operations is a key factor. After the latching phenomenon occurs, current flow naturally stops, preventing static power dissipation in the current-sensing amplifier [1]. Consequently, the delay in detection and latching is closely linked to power dissipation. Since memory occupies around 90% of a chip's surface area, power dissipation within on-chip cache memory contributes significantly to the overall power consumption of the memory chip [2]. The most commonly used sense amplifier in SRAM ICs is the CMOS Cross-Coupled Inverter, where the input and output lines operate simultaneously. This design results in higher time delays and power dissipation. However, latch-type sense amplifiers, due to their high input impedance, reduce these issues [3]. Sense amplifiers can be categorized as voltage-based or current-based, depending on the type of signal applied to the input. A voltage sense amplifier requires a voltage change on the bit-line before it can detect and amplify the voltage difference to the full swing range. As technology progresses, the decision span increases, and voltage swing decreases to micron or submicron levels. In contrast, a current

sense amplifier amplifies the smallest differential signal from bit-lines or data lines, outputting it at CMOS logic levels. Its lower input impedance makes it one of the most effective solutions for reducing both sensing delay and power consumption in SRAM [4]. This paper presents a comparative study of various current and voltage sense amplifiers. The novelty of this work lies in its explanation of the underlying causes of delay and power dissipation in the respective types of sense amplifiers.

2. TYPES OF SENSE AMPLIFIER (SA)

(i) STANDERD SENSE AMPLIFIER

The average power consumption of standard sense amplifier implementations was evaluated using 90 nm MOS technology. Figure 1 shows the schematic of the basic latch sense amplifier design, while Figure 2 illustrates its power consumption spectrum. This sense amplifier is optimized for fast differential signal detection on the bit-lines, aiming to improve throughput while minimizing power consumption, which remains around 7.2 mW.

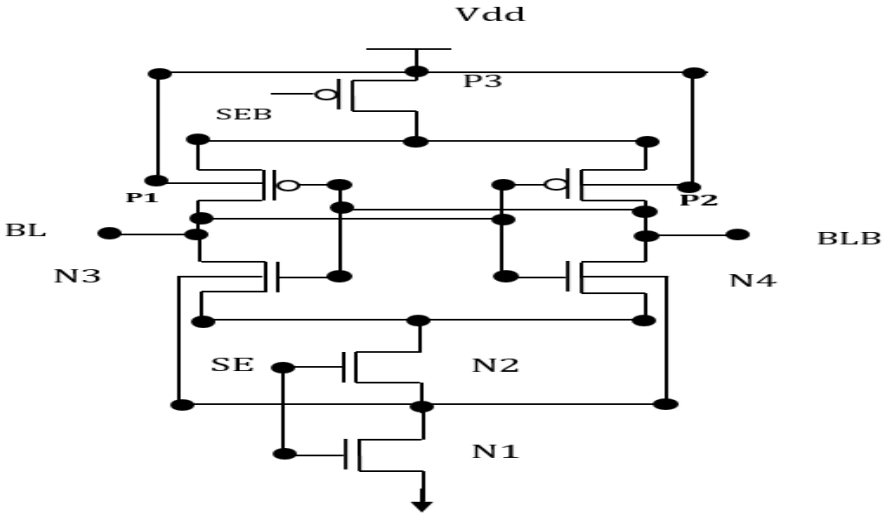

Figure 1: Schematic of Standard Latch Sense Amplifier

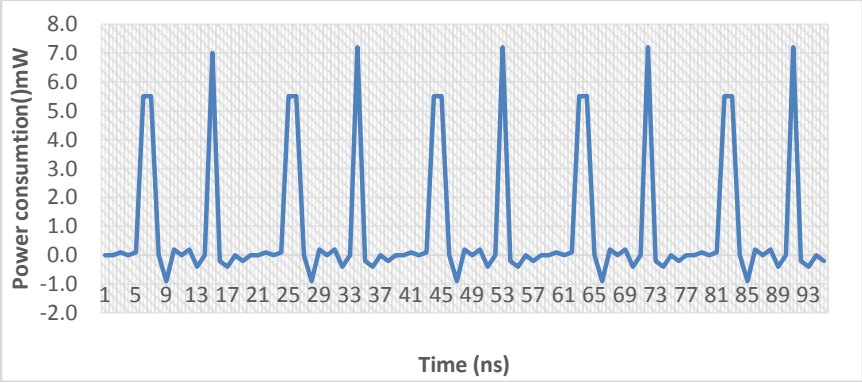

Figure 2: Power Consumption Waveform of Basic Latch Sense Amplifier

(ii) STANDERD SENSE AMPLIFIER

The introduction of pass transistors in the basic latch sense amplifier design, shown in Figure 3, isolates the amplifier inputs and outputs from the bit-lines. This modification prevents the sense amplifier from erroneously reading the SRAM value stored in the cell after the bit-lines have fully discharged, a potential issue in the previous design where the bit-lines and sense amplifier shared physical nodes. While this updated design with pass transistors benefits from distinct physical node separation, the addition of two NMOS transistors on each side introduces a voltage drop, as depicted in Figure 4. This voltage drop could lead to biased logic values due to variations in transistor sizing during fabrication.

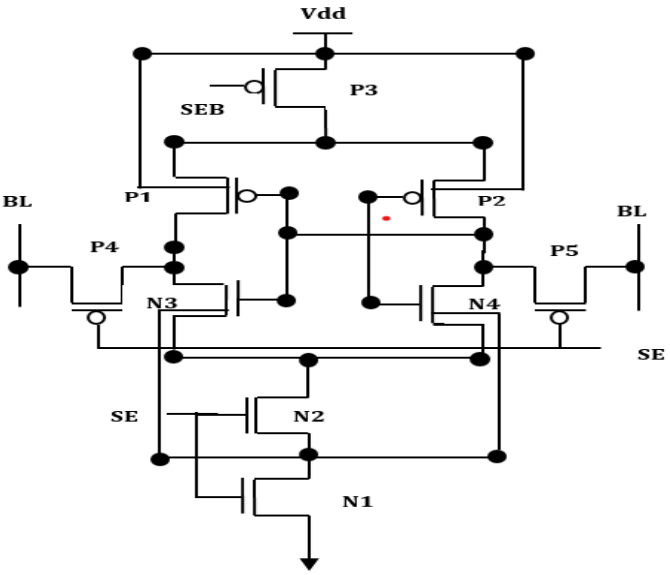

Figure 3: Schematic of Basic Latch Sense Amplifier

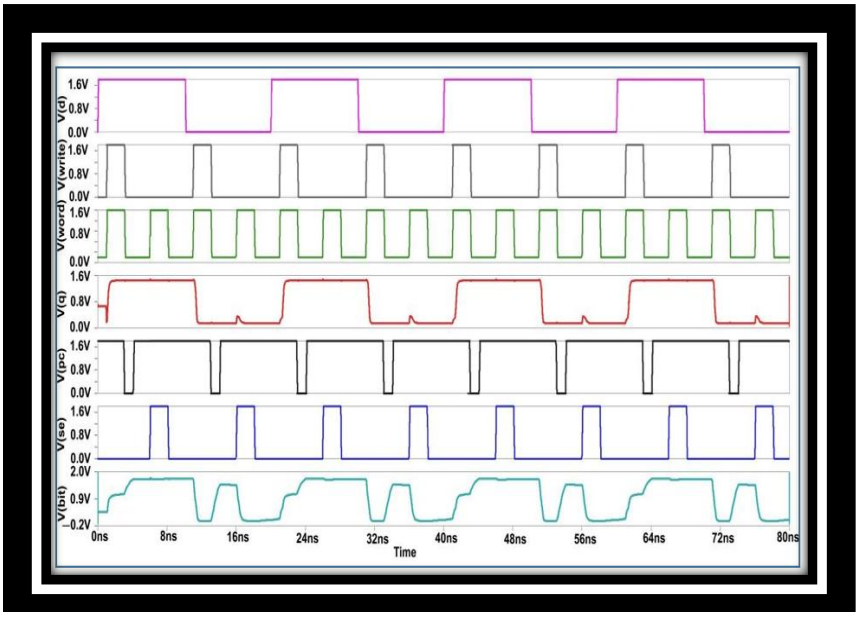

Figure: 4: Output waveform of Latch Sense Amplifier

(iii) STANDERD SENSE AMPLIFIER

Figure 5shows the cross-coupled sense amplifier configuration, highlighting the "Sensing Enable (SE)" signal's shared link. Because of this scheme, fewer transistors are required for independent write and sensing enable signals. As a result, the power consumption drops to 0.8 mW at 90 nm, as seen in Figure 6.

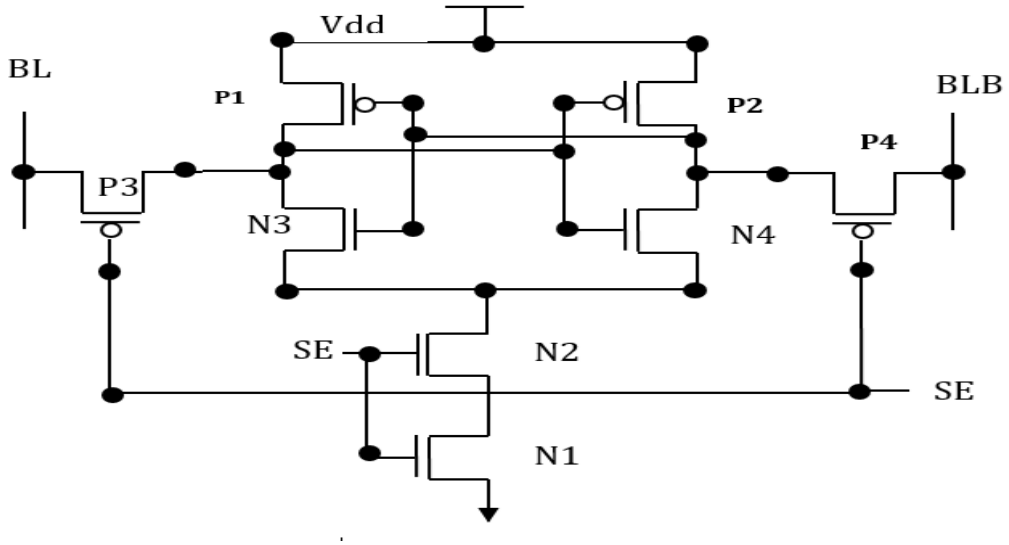

Figure 5: Schematic of Cross Coupled Sense Amplifier

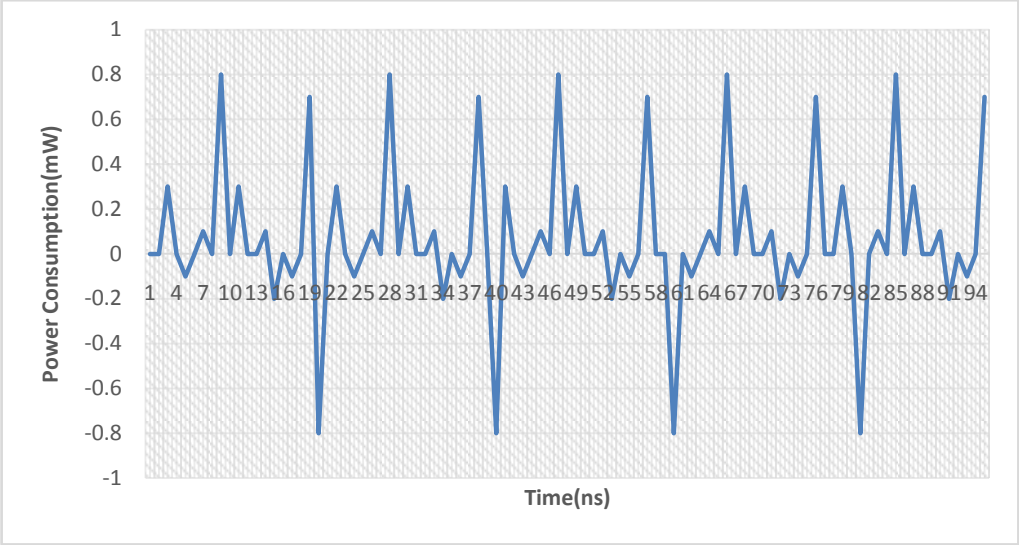

Figure 6: Power Consumption Waveform of Cross-Coupled Sense Amplifier

Comparative performance of average power consumption and related transistor sizes for the three traditional designs are summarized in Table 1. Furthermore, the power reduction strategies of source biasing and negative word-line that we used in our suggested design were also used in the traditional designs. Transistor sizes and the resulting power readings were noted and shown in Table 1.

(3)PROPOSED DESIGN OF SENSE AMPLIFIER

According to the detailed description of sense amplifiers, it is confirmed that the main function of sense amplifiers is to amplify the tiny voltage differential between bit-lines into a logically high value. The substantial capacitive load carried by the bit-lines causes RC delays. Recent developments in SRAM designs [17–26] highlight novel device architectures that claim lower power consumption, including 6T SRAM with FinFETs, Memristors, and Junction less TFETs. Accordingly, we optimize energy economy by including power reduction approaches into our suggested sense amplifier architecture.

Furthermore, as previously noted in previous designs, sense amplifiers use a differential logic circuit to improve the logic circuits' complexity and decrease the latency that the differential circuit experiences [13]. Huge-scale SRAM design with CMOS technology is a significant difficulty because these huge SRAMs require a large number of bit-lines, which causes significant delays [11].Fast sensing is the main objective, although it is hampered when designs run at voltages lower than the supply voltage [4]. One of the most popular designs is the cross-coupled sense amplifier, which has a complimentary structure made up of two pull-up and two pull-down transistors. Cross-coupled capacitance and discharge conductivity values determine this design's speed and loading characteristics. It is noteworthy that conductivity and capacity have an inverse relationship, with more conductivity resulting from lower capacity. As seen in Figure 7, the suggested design substitute’s two transistors for the two cross-coupled inverters. Transistors N4 and N5 activate in response to word-line activation, enabling the bit-line voltage to reach the output terminals.Source biasing is a technique used to reduce leakage current in order to further minimize power consumption. An NMOS transistor is added to the circuit's end for source biasing. It is controlled by the sense enable signal and, when it is triggered, produces a virtual ground. A pull-down NMOS transistor is inserted between the SRAM cell's ground and source lines, with its gate terminal coupled to the word-line, in order to reduce leakage current and save power [4]. In active mode, the word-line going high triggers the transistor to turn on. Normal SRAM cell operation is made possible by the virtual ground voltage (VSL), which works as a genuine ground line because of its low resistance. The source voltage rises in standby mode when the WL is reduced and N4 is turned off, which lowers sub-threshold and gate leakage currents.For big memories, we find that power-saving techniques also result in shorter access times. The bit-lines in the suggested architecture suffer from less capacitance effects, which lowers the RC delay, thanks to the combination of the cross-coupled FET configuration with negative word-line and source biasing approaches. The "Modified Cross-coupled design" shown in Figure 8 makes this clear. Going back to our suggested design, we incorporated the negative bit-line approach during READ mode, which functions similarly to source biasing by providing a negative voltage to the word-line during idle times without affecting Soft Error Rate (SER) or device performance [4]. The sub-threshold leakage current is greatly decreased by this approach since the access transistors are shut off. The potential increase in gate leakage current of the access transistor as a result of wider gate-source and gate-drain voltage differences is a disadvantage of this method. The write signal value is essentially stabilized within a certain range by this method. Power consumption is therefore significantly reduced by integrating these two designs into the altered configuration.

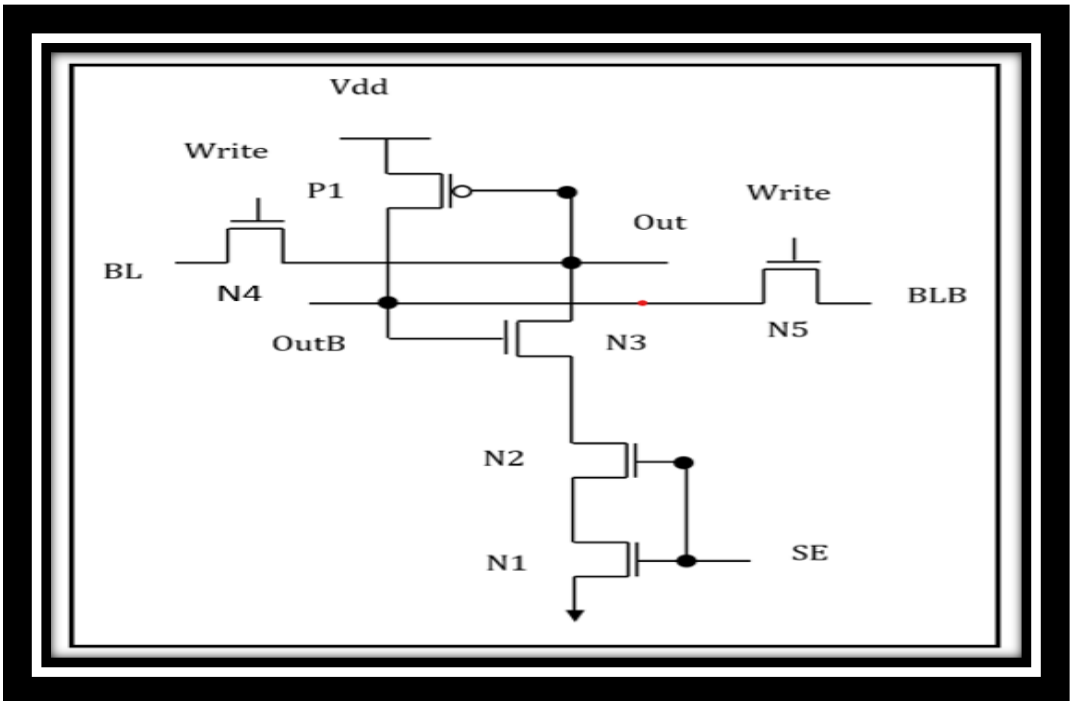

Figure 7: Schematic of Proposed Design of Modified Cross-Coupled SRAM

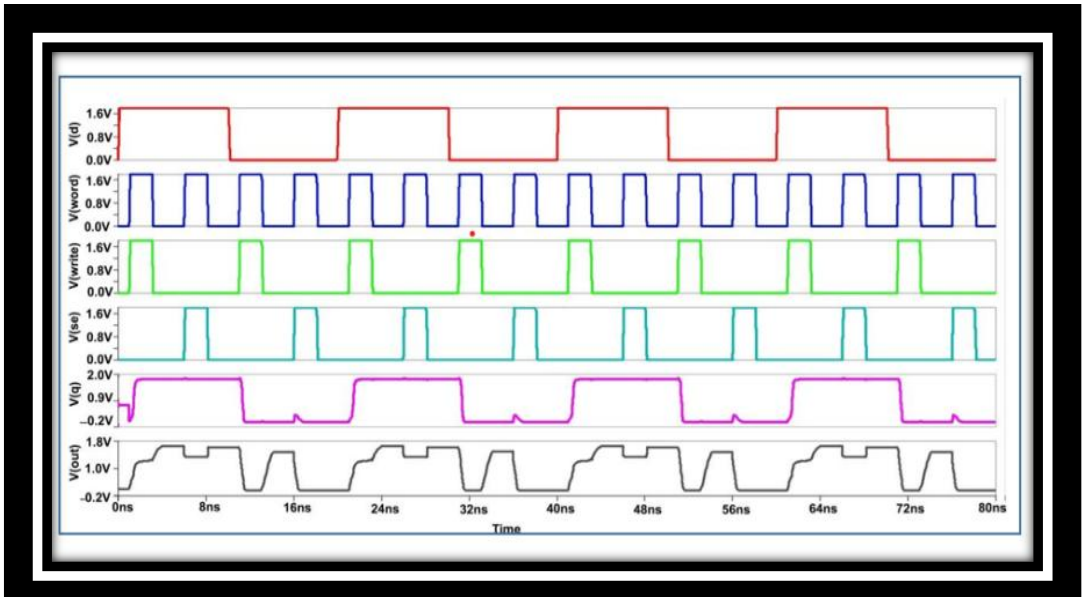

Figure 8: Output Waveform of Proposed Sense Amplifier

The proposed sense amplifier arrangement in static RAM's hold, read and write Static Noise Margin (SNM) tests are shown in Figures 9 and 10. The suggested device's strong noise resilience, which is essential for guaranteeing precise SNM window frames during read and write operations, is confirmed by these results.Better signal quality is indicated by a larger noise margin. A few microsecond pulse width is exceptionally long for high-speed ICs compared to the propagation delay time of the circuit. Consequently, the Modified Cross-Coupled sense amplifier is more suited for constructing high-speed SRAM circuits due to the reduced delay caused by the reasonable noise margin attained in the suggested design.

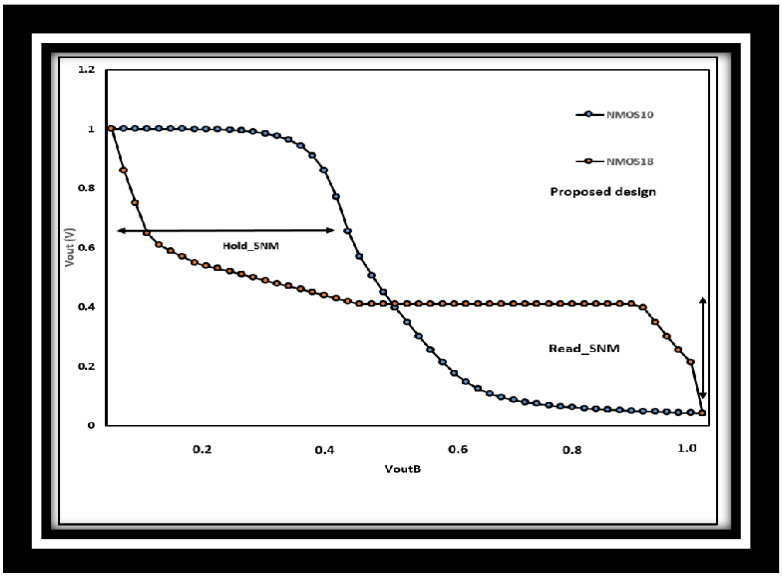

Figure 9: Hold and Read static noise margin of proposed design

Data is moved from data D to data Q during the write cycle when the write and word signals are both set to HIGH input (logic 1) at the same time. We start the read cycle by turning on the SE (sensing enable) and pre-charging the circuit. The NMOS transistor fails to transmit a perfect or strong 1 when a logic 1 is written to the left side of the SRAM cell, preventing the bit-line from reaching full charge to VDD. The bit-line on the other side is fully charged to zero, but the transistors' threshold voltage causes two voltage drops at the Q output.

Toggling the cell to the required state only requires this difference. The PMOS transistor can send a full or strong 1 when the PC (pre-charge) signal is set to logic 0, which fully charges the bit-lines to VDD. For the read operation, the data must be copied from the Q output to the bit output by simultaneously setting the word-line and SE signal to HIGH logic [9].

As indicated in the "modified" column, Table 1 lists the power reduction strategies used in the traditional designs. In every scenario, the source-biased transistor's addition lowers power usage. With an average power consumption of 7.5912 µW, the redesigned cross-coupled sense amplifier is comparable to the 7.0015 µW power consumption of our suggested design. The transistor size area is lower in our suggested design, though, which makes it the best option for a low-power, high-performance sense amplifier that is perfect for high-speed SRAM applications.

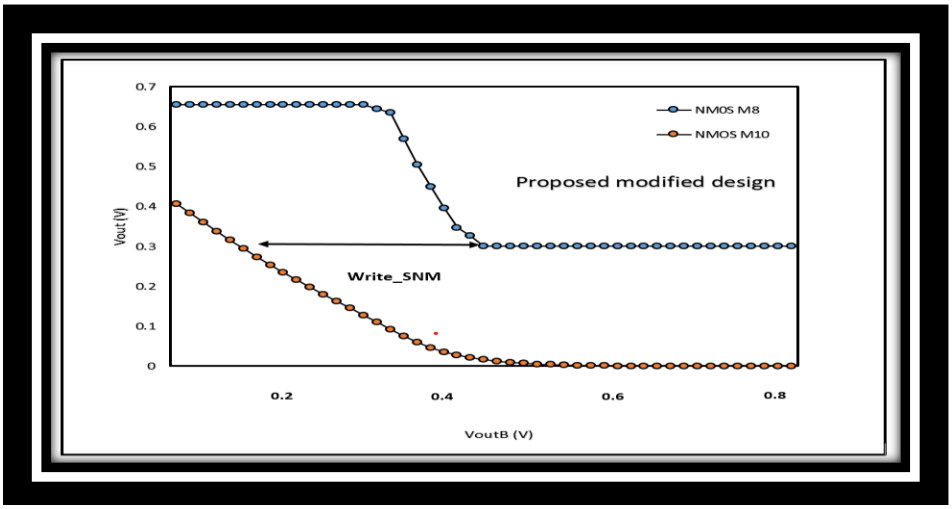

Figure 10: Write static noise margin of proposed design

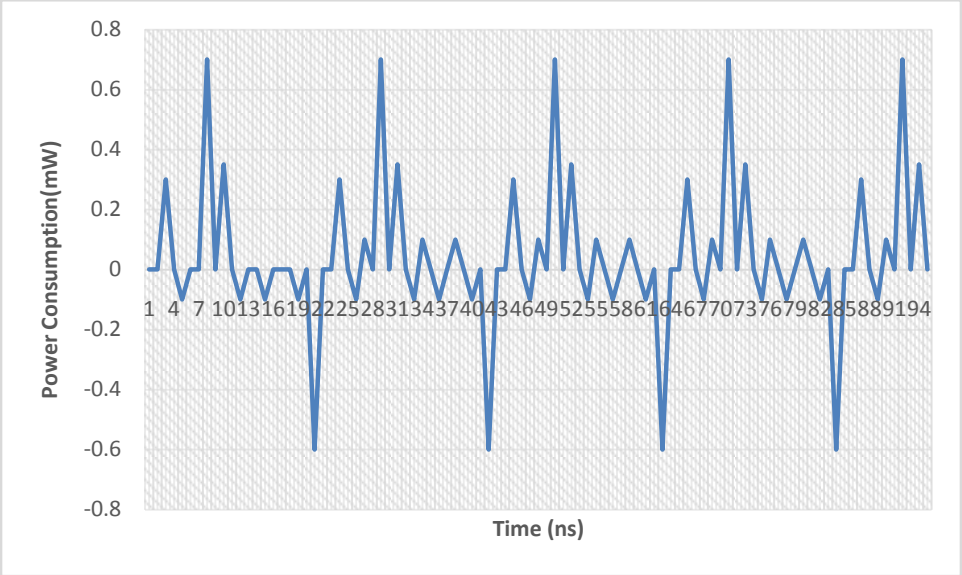

Figure 11: Power consumption spectrum of proposed Sense Amplifier

Table 1: Average power consumption of various Sense Amplifier

S. No.	Sense Amplifier Name	No. of Transistors	Power Consumed (µW)	No. of Transistors (Modified)	Power Consumed (µW)
1	Basic Standard Latch Sense Amplifier [**9**]	6	80.713	7	39.504
2	Basic Latched Sense Amplifier [**1**]	8	81.061	9	9.46
3	Cross Couple sense Amplifier [**10**]	7	77.097	8	7.5912
4	**Proposed Design**	**5**	**78.00**	**6**	**7.0000**

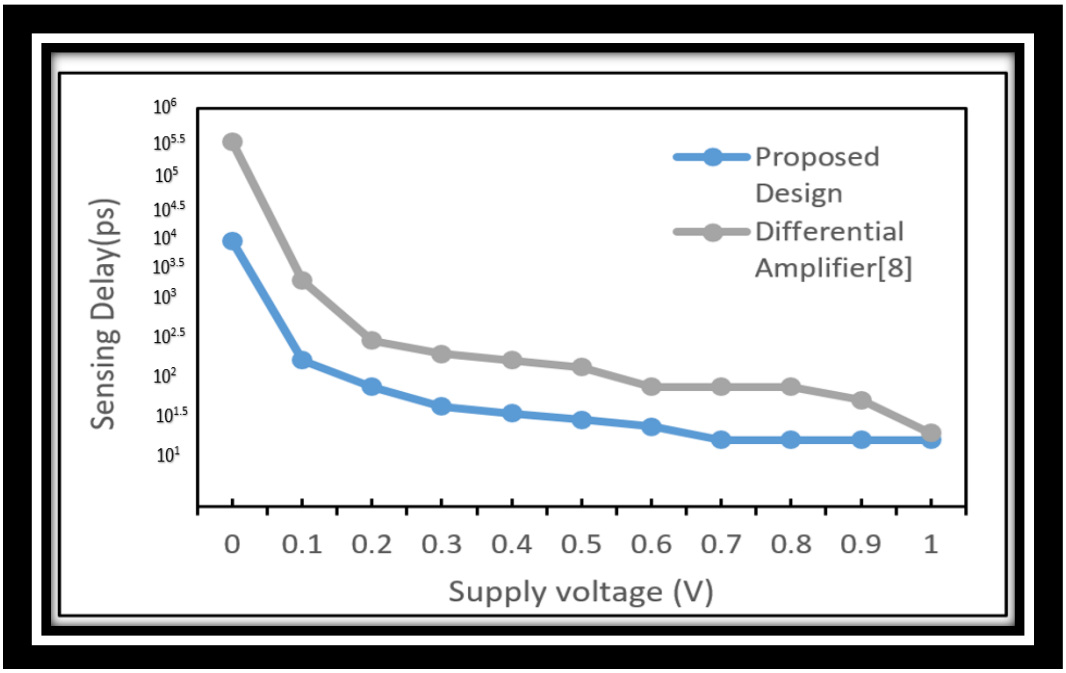

Figure 12: Sensing delay performance of Sense Amplifier

Figure 12 illustrates how the overall sensing delay has a significant impact on the sense amplifier's performance. The suggested Modified Cross-Coupled SRAM architecture exhibits a lower sensing delay in comparison to the differential sense amplifier by utilizing negative bit-line and source biasing techniques [8]. The reduced capacitance effect on the bit-lines, which results in a large reduction in latency, is responsible for the suggested design's notable (almost 99%) drop in sensing delay at an initial supply voltage of 0.1 V. By supplying a negative voltage to the word-lines, the capacitance effect is reduced while preserving the integrity of the delay, power, and noise margin. From 5.5 ns to 55 ps, the sensing delay reduces when the supply voltage fluctuates between 0.1 V and 1.0 V.

1. REFERENCES

2. K. Soundrapandiyan, S. K. Vishvakarma and B. S. Reniwal, "Enabling Energy-Efficient In-Memory Computing with Robust Assist-Based Reconfigurable Sense Amplifier in SRAM Array," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 13, no. 1, pp. 445-455, March 2023, doi: 10.1109/JETCAS.2023.3243192.
3. J. Chen, W. Zhao, Y. Wang and Y. Ha, "Analysis and Design of Reconfigurable Sense Amplifier for Compute SRAM With High-Speed Compute and Normal Read Access," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 12, pp. 3503-3507, Dec. 2021, doi: 10.1109/TCSII.2021.3123512.
4. B. Rawat and P. Mittal,"A 32 nm single- ended single-port 7T static random-access memory for low power utilization. Semiconductor Science and Technology," vol. 36, issue 9, pp. 6–22, 2021, DOI: 10.1088/1361-6641/ac07c8.
5. C. Kishore and A. Kumar, "Comparative Analysis of Various Sense Amplifiers in 45nm CMOS Technology," *International Research Journal of Engineering and Technology*, vol. 6, issue 5, pp.102–106, 2019.

6.Kobayashi,T.;Nogami,K.;Shirotori,T.;Fujimoto,Y.Current-ControlledLatchSenseAmplifierandaStaticPower-SavingInputBufferfor Low-PowerArchitecture.*IEICETrans.Electron.***1993**, *76*, 863–867.[CrossRef]

7.R. Selvakumar, M. Lakshmana Kumar and S. Raja Gopal, "Material analysis of high degree of variability in thin CMOS for SRAM current sense amplifier,"*Materials Today: Proceedings*, vol. 21, Part 1, 2020, pp. 299-306, Doi:10.1016/j.matpr.2019.05.444.

8.Conte,A.;Giudice,G.L.;Palumbo,G.;Signorello,A.AHigh-PerformanceVeryLow-VoltageCurrentSenseAmplifierforNonvolatile Memories.*IEEEJ.Solid-StateCircuits***2005**,*40*, 507–513.

9.Jeong,H.;Kim,T.;Kang,K.;Song,T.;Kim,G.;Won,H.S.;Jung,S.O.SwitchingPMOSSenseAmplifierforHigh-DensityLow-VoltageSingle-EndedSRAM.*IEEETrans.CircuitsSyst.IRegul.Pap.***2015**,*62*,1555–1563.

10. Yoon,T.;Park,J.;Jeong,H.DesignofStaticRandom-AccessMemoryCellforFaultTolerantDigitalSystem.*Appl.Sci.***2022**,*12*, 11500.

11. Patel,D.;Neale,A.;Wright,D.;Sachdev,M.BodyBiasedSenseAmplifierwithAuto-OffsetMitigationforLow-VoltageSRAMs.*IEEETrans.CircuitsSyst.IRegul.Pap.***2021**,*68*,3265–3278.

12. Kumar, PawarDhiraj, Ritesh Kumar Kushwaha, and P. Karuppanan. "Design and Analysis of Low-Power SRAM." Advances in VLSI, Communication, and Signal Processing: Select Proceedings of VCAS 2019. Springer Singapore, 2021.

13. Kim, Youngbae, "Ultra-low power and high-throughput SRAM design to enhance ai computing ability in autonomous vehicles." Electronics 10.3 (2021): 256.

14. Dutt, Divya, "Design and performance analysis of high-performance low power voltage mode sense amplifier for static RAM." Advances in Electrical and Electronic Engineering 20.3 (2022): 285-293.

15. Chen, Jian, "Analysis and design of reconfigurable sense amplifier for compute SRAM with high-speed compute and normal read access." IEEE Transactions on Circuits and Systems II: Express Briefs 68.12 (2021): 3503-3507.

16. Saini, Aarti, Parnav Kumar Gupta, and Ruchi Gupta. "Analysis of low power SRAM sense amplifier." 2019 International Conference on Electrical, Electronics and Computer Engineering (UPCON). IEEE, 2019.

17. Saun, Shikha, and Hemant Kumar. "Design and performance analysis of 6T SRAM cell on different CMOS technologies with stability characterization." IOP conference series: materials science and engineering. Vol. 561. No. 1. IOP Publishing, 2019.

18. Shukla, Neeraj Kr, Pulkit Bhatnagar, and Shilpi Birla. "Design and Analysis of a Novel Ultra-Low Power SRAM Bit-Cell at 45nm CMOS Technology for Bio-Medical Implants." International Journal of Computer Applications 975: 8887.

19. Mishra, K. Chandra, and R. K. Singh. "Design and Analysis of Low Power SRAM using CMOS Technology'." Int. J. Innov. Technol. Explor. Eng 8.12S (2019): 896-902.

20. Dounavi, Helen-Maria, YiorgosSfikas, and YiorgosTsiatouhas. "Periodic monitoring of BTI induced aging in SRAM sense amplifiers." IEEE Transactions on Device and Materials Reliability 19.1 (2019): 64-72.