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A STUDY ON LOW-POWER ALU DESIGN LEVERAGING VARIOUS ADVANCED OPTIMIZATION METHODS

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Abstract: VLSI technology has advanced significantly, and there are numerous effective methods for creating VLSI circuits. PTL, GDI (Gate Diffusion Input) methods, and CMOS are a few of the styles. The weaknesses of CMOS and PTL approaches can be eliminated by using the GDI technique to create low-power digital combinatorial circuits. This method maintains a low level of logic design complexity while lowering the amount of power consumed, propagation latency, and size of digital circuits. This paper discusses the benefits and limitations of GDI compared to CMOS design by comparing the various approaches with respect to layout area, transistor count, latency, and power dissipation.

Keywords: CMOS, Gate Diffusion Input (GDI), Pass Transistor Logic (PTL), Propagation delay,low-power.

1. INTRODUCTION

The increased focus on high-speed, low-power embedded systems for smart phones, laptops, and other devices has caused VLSI technology to shrink to nanoscale levels, enabling the integration of more functionality onto a single chip. Over the past 20 years, a number of logic design methodologies have been developed in response to the desire to enhance the performance of logic circuits, which were previously based on conventional CMOS technology [6] [2, 3Pass-transistor logic (PTL) is a popular type of logic used in low-power digital circuitry. For nMOS, formal techniques for obtaining pass-transistor logic have been provided. They are based on the model in which the gates of nMOS transistors are subjected to a series of control signals. The sources of the n-transistors are subjected to an additional set of data signals. For low power digital circuits, the PTL (Pass Transistor Logic) is most commonly used.

PTL has several advantages over traditional CMOS design, including: 1) high speed because of small node capacitances; 2) low power dissipation since fewer transistors are used; and 3) less connectivity effects because of a compact area. But there are two main issues with PTL implementation: 1) Low drive current due to the single channel pass transistor's threshold voltage drop causes slow operation at lower power supplies; 2) significant direct path static power dissipation occurs because the regenerative inverter's high input voltage level is not V_{dd} and the PMOS device is not fully turned off. GDI is a technique that, in comparison to conventional CMOS design and current PTL techniques, is appropriate for designing quick, low power circuits with fewer transistors.

1.1 ARITHMETIC LOGIC UNIT (ALU)

Inside the central processing unit (CPU) of every digital computer, the Arithmetic Logic Unit (ALU) functions as the heart. The ALU's job is to process data using logic and arithmetic

before sending it to the computer's memory. Power consumption will become a major issue as technology advances and design complexity rises since there are more transistors in use, which means that integrating them requires more energy and power [27]. Power dissipation is made up of two basic components, as demonstrated by equation 1 [28]. These are static and dynamic power dissipation. Furthermore, additional The use of transistors in Very Large-Scale Integration (VLSI) design will also result in an increase in area and a slight delay in the output execution [29].

$$\mathbf{P_{avg\ power} = P_{dynamic\ power} + P_{static\ power}}$$

The following operations are performed by an arithmetic unit: addition, addition with carry, subtraction, subtraction with borrow, and transfer functions. Initially, we create a single-bit Full Adder, followed by a 4-bit Ripple Carry Adder with four Full Adder numbers, and finally a 32-bit Ripple Carry Adder with eight 4-bit Ripple Carry Adder numbers. Next, we created a singlebit 4:1 multiplexer with 32 numbers. Fig. 6 displays the schematic of a 32-bit Arithmetic Unit. The circuit contains thirty-two multiplexers and a 32-bit parallel adder to create a 32-bit arithmetic unit[5].A and B are the two 32-bit inputs, while RESULT is the 33-bit output. Every multiplexer has a 4:1 size. S0 and S1 are the two common selection lines shared by all thirty-two multiplexers. The parallel adder's carry out is Cout, and its carry input is C_in. Each multiplexer has thirty-two inputs: logic-0, logic-1, B-value, and Complemented B-value. The following arithmetic sum is used to calculate the circuit's output[26].

RESULT = A + Y + Cin

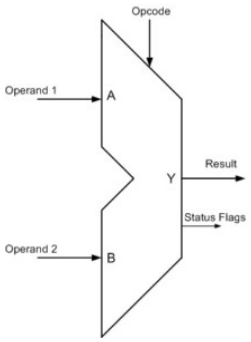

Figure1. ALU Symbol

In this CMOS technology, both N-type and P-type transistors are used to realize logic functions. The N type and P type transistor are used for turns on and turn off a transistor. The design used simple switches. In this paper CMOS logic gates a collection of n-type MOSFETs is arranged in a pull down network (Vss or ground). In place of load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network, higher voltage rail (often named Vdd)[1]. Thus, if both a p-type and n-type transistor have their gates connected to the input, the p-type MOSFET will be on when the n-type MOSFET is off, and vice-versa as shown in the fig. 6 .In CMOS, when the input is high, NMOS gets ON and pulls down the output to ground(i.e., output becomes low). Whereas, when the input voltage is low, PMOS gets ON and pulls the output up from the ground (i.e., output becomes high). So we call PMOS as PULL UP transistor and NMOS as PULL DOWN transistor.

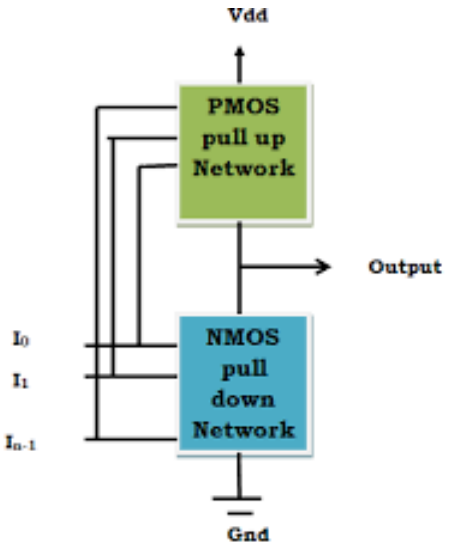

Figure 2.pullup and pull down

2. SOURCES OF POWER CONSUMPTION IN CMOS CIRCUITS

1. Short Circuit Power Consumption
2. Dynamic Power Consumption
3. Leakage(Static) Power Consumption

2.1 Short Circuit Power Consumption:

This results due to direct path short circuit current which arises when both NMOS & MOS are simultaneously active and conduct current through resistive path between source and ground

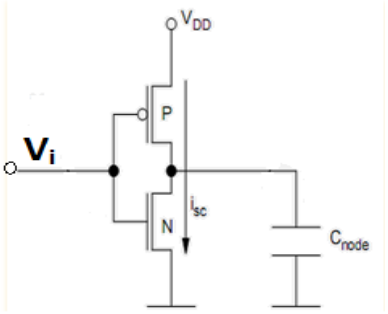

Figure 3: Short circuit

Short Circuit Power Psc = Isc * Vdd

Isc= short circuit current

Vdd=supply voltage

2.2Dynamic Power Consumption:

Dynamic power consumption in CMOS circuit is due to charging and dis-charging of load capacitance

Dynamic Power :

P_{dyn} =1/2 CLVdd2 α f

CL = load capacitance

V_{dd} = Supply voltage

f= frequency

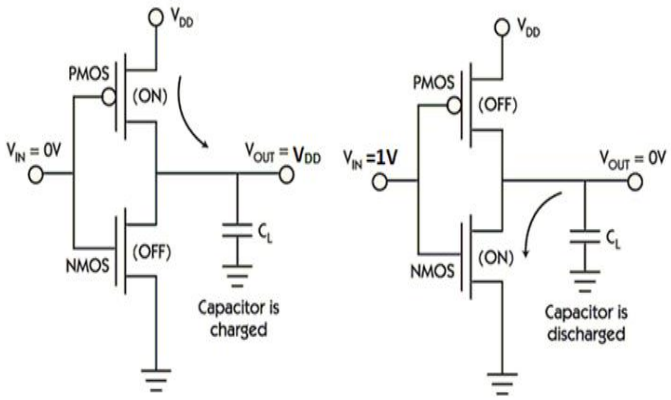

Figure 4: Dynamic circuit

2.3:Leakage Power Consumption:

This power consumption takes place due to the flow of leakage currents through the device when it is in idle state.

Leakage Power Pleak = I_{leak}* V_{dd}

$I_{leakage}$= Leakage current, V_{dd}=Supply voltage

Total power consumption= P_{sc} + P_{dyn} + P_{leak}

3. DESIGN TECHNIQUES

3.1 CMOS Technique:

The acronym for a complementary metal oxide semiconductor is CMOS. It uses transistors that are both PMOS and NMOS. PMOS transistors make up the pull-up network, and NMOS transistors make up the pull-down network. Electronic devices used PMOS and NMOS separately before CMOS. Among these, NMOS gained traction because of its quick functioning and cheaper price as compared to PMOS. One of NMOS's drawbacks is that it uses more static power. Circuit design is made more flexible when NMOS and PMOS are combined symmetrically in a single integrated circuit. Another benefit of CMOS is its low power consumption—it uses practically no power when it is in a static state. Transistor size, resilience, and dependable operation at low speeds are benefits of CMOS logic[4]

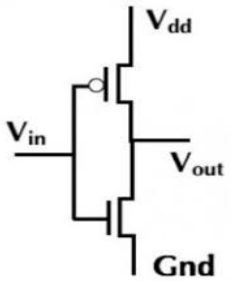

Figure 5. Basic CMOS cell

3.2 GDI and m-GDI Technique:

GDI stands for Gate Diffusion Input. This design technique is used for reducing power in circuits. Along with power it also reduces the area of the circuit. The various logic functions such as AND, OR, etc. can be realized using only two transistors, one PMOS and one NMOS. The logic operations that can be implemented using a basic GDI cell are listed in the Table I.

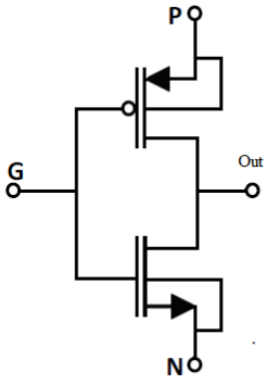

Figure 6: Basic GDI cell

Table 1 Logic functions realized using basic GDI cell

N	P	G	OUT	Function
0	B	A	AB	F1
B	1	A	A+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	AB+AC	MUX
0	1	A	A	NOT

The GDI technology is modified and called m-GDI. This maintains the potential of all body terminals, meaning that the bodies of all PMOS and NMOS are connected to VDD and VSS in the proper manner.

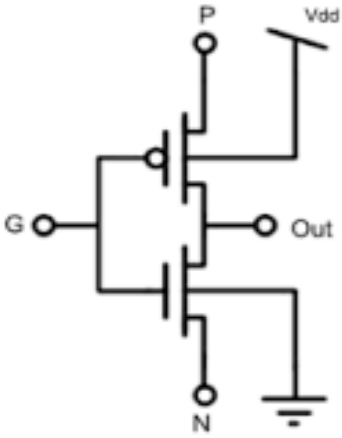

Figure 7: Basic m-GDI cell

One limitation of the GDI and m-GDI techniques is that full swing output voltage cannot be achieved. The FS-GDI Method Full Swing Gate Diffusion Input is known as FS-GDI. It is a low power design strategy that minimises power usage and delays.

Compared to CMOS technology, full swing GDI technology operates more quickly [3]. This technology uses less transistors than the CMOS technique, even if it uses more than the m-GDI technique. It is a method for improving the output swing that is derived from the m-GDI method. It is used instead of swing restoration buffers to provide full swing output [4].

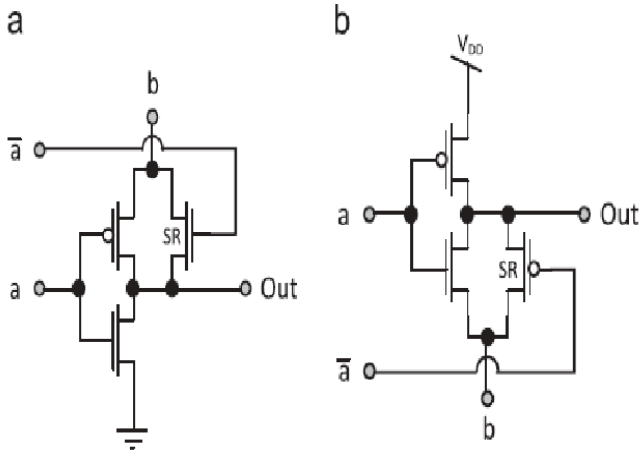

Figure 8: Basic FS-GDI cells

4. PREVIOUS WORK

Some of the techniques to reduce power consumption in CMOS circuits are

1. Power gating
2. Clock gating
3. Transistor Sizing
4. Multi threshold technique
5. Variable threshold CMOS technique

It is possible to produce power decreasing at the circuit, module, or architectural levels [2]. Select information reason as the control rationale in a basic switch method, allowing additional information signal from the gate terminal [3]. An essential structure for ALU planning is the Full Adder. There are other types of FA planning that can be used in place of limiting forces, such as the 11 transistor FA (11T-FA), 10 transistor reduced power Full Adder (10T-FA), and Hybrid Full Adder (H-FA). FA operates in ultra-low mode with reduced power consumption by using subthreshold current [2], [3]. A 2:1 multiplexer and an XOR gate with close to ground power are used in the manufacturing of full adders. An ALU arrangement using the FinFET breakthrough features two electrically free gates. This reduces the circuit's complexity and, as a result of the leakage current decreasing, also lowers power consumption. The term "Fin" in Fin Field Effect Transistor (FinFET) invention refers to the thin silicon that forms the device's frame [4]. The Multiple Input Floating Gate - Metal Oxide Semiconductor (MIFG-MOS) transistor's re-configurable logic is used in the Arithmetic Logic Unit plan. This circuit's effectiveness is increased by a multitude of information. By monitoring the weighted sum of all factors taken into consideration, the MIFG-MOS transistor provides low and high situations. In addition to enhancing the circuit's display, MIFG-MOS transistors reduce the number of transistors and the circuit's unpredictable nature. They also restrict power distribution and delay [5]. When channel size scaling

becomes unfavourable for circuit organisation, metal gates and dielectric K values greater than or equal to those should be promoted.

In [9] the authors have designed Power gated ALU. In [10] the authors have developed Low power arithmetic logic unit based sliced processor using GDI and MGDI, In [11] the authors have implemented FS-GDI approach with 65 nm technology for low power ALU, In [12] the authors have performed 8-Bit ALU Design using m-GDI Technique, In [13] the authors have simulated 8-bit ALU design using GDI techniques with less power and delay, In [14] the authors have proposed implementation of ALU using grapheme nano ribbon field-effect transistor and fin field-effect transistor, In [15] the authors have done MWCNTB On-chip Interconnects for ALU designed, In [16] the authors have designed 16-bit ALU Using Full-Swing GDI, In [17] the authors have analysis of ALU using Full Swing GDI Technique, In [18] the authors have done Performance Efficiency Analysis of ALU, In [19] the authors have Simulated Optimized Low Power ALU of 4-Bit Processor using 32nm Technology, In [20] the authors have done ALU Implementation Using CMOS Technology, In [21] the authors have provided Analysis of 8-Bit Low Power ALU in 45 nm Using GDI Technique, In [22] the authors have developed High Speed ALU in 45nm Using GDI Technique, In [23] the authors have designed ALU using VHDL for low power, In [24] the authors have implemented low power Brisk architecture of ALU, In [25] the authors have focused on building a Low Powered ALU with the implementation of Built-In Self-Test(BIST) mechanism for efficient arithmetic. and logical operations.

S.No	Title	Technique	Power consumption	Delay
1	Power and Delay Optimization of 8-Bit ALU using Various Techniques	CMOS	67.62x10-6	0.0635x10- 6
		TG LOGIC	34.86x10-6	0.0285x10- 6
		GDI LOGIC	32.45x10-6	3.5695x10- 6
		MGDI LOGIC	16.51x10-6	0.0013x10- 6
		FSGDI LOGIC	12.23x10-6	0.0066x10- 6
2	Design of PTL based Area Efficient and Low Power 4-bit ALU	PTL	2.58E+02	4.60E-10
		CMOS	1.20E+01	8.63E-10
3	Design and Analysis of 8-Bit Low Power ALU in 45 nm Using GDI Technique	CMOS	1139.84	3.9399
		GDI	510.08	2.2229
4	Design of 4 Bit ALU Using Modified GDI Technology for Power Reduction	GDI	0.214	0.933(ns)
		m-GDI	0.091	1.486(ns)
5	8-Bit ALU Design using m-GDI Technique	m-GDI	31.57 (uW)	4.57 ns)

CONCLUSION

Static power dissipation and dynamic power dissipation are the two categories into which power consumption in CMOS circuits is divided. Static power dissipation is not taken into consideration in today's CMOS circuits since it is so small in comparison to dynamic power dissipation. Dynamic power is intimately correlated with the power supply. With GDI implementation, there are fewer power supply to ground connections, which lowers dynamic power usage. This study examines and contrasts several methods for lowering the power consumption of ALU circuits. Of all the design strategies, the GDI technique turned out to have the best performance characteristics.

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