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Exploring Partial Adiabatic Logic Techniques for Low-Power VLSI Circuit Design: A Review

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Abstract: As CMOS technology scales down, challenges like leakage currents and power dissipation intensify, making low-power strategies essential. Optimizing energy efficiency while maintaining performance is essential for low-power digital circuits. The need for logic devices that use minimal power is continually growing and adiabatic logic provides a promising solution, being classified into Partial Adiabatic Logic (PAL) and Fully Adiabatic Logic (FAL). PAL circuits offer significant power savings compared to traditional CMOS (Complementary Metal-Oxide Semiconductor) circuits while balancing efficiency and speed. This paper reviews PAL techniques, focusing on its principles, design methodologies, and operational characteristics. simulations of inverter circuits using techniques like ECRL (Efficient Charge Recovery Logic), PFAL (Positive Feedback Adiabatic Logic), etc. are presented, comparing their performance with CMOS logic across varying supply voltages and clock frequencies. Key metrics such as power dissipation, propagation delay, and energy savings are analysed. Results show that DCPAL and DC-DB PFAL achieve power savings of up to 88.8% and 76%, respectively. Challenges in PAL implementation and future research directions are discussed. Simulations using cadence virtuoso highlight PAL's potential for energy-efficient applications in IOT, biomedical devices, and mobile electronics.

Keywords: adiabatic logic, CMOS, FAL, low-power, power clock, PAL.

1. INTRODUCTION

In recent years, the rapid advancement of Very-Large-Scale Integration (VLSI) technology has fueled the development of increasingly complex and power-hungry digital circuits. As power dissipation becomes a significant challenge, especially in mobile, wearable, and Internet of Things (IoT) devices, there is an urgent need for innovative low-power design techniques. Traditional methods, such as multi-threshold CMOS and dynamic voltage scaling, have been instrumental in reducing power consumption; however, they are reaching their limits due to the physical constraints imposed by scaling down transistor sizes in modern CMOS technology. The growing demand for energy-efficient digital circuits has become a major focus in today's electronics industry. As electronic devices continue to pervade a wide range of sectors, from portable gadgets to data centers[1], the need to optimize power consumption has intensified. This drive is fueled by several factors, including the need to extend battery life in mobile devices, reduce environmental impact, and achieve economic gains through lower energy usage[2]. As a result, power consumption has become a critical design parameter for all digital integrated circuits (ICs), where achieving a balance between power efficiency and performance is crucial to meeting system demands[3].

In particular, the quest of high performance in VLSI circuits has led to a sharp increase in power consumption due to the frequent switching of transistors which has emerged as a significant concern for VLSI designers. Moreover, excessive power dissipation can lead to IC packaging challenges and reliability issues[4]. Given the global energy crisis, researchers are increasingly focused on developing low-power techniques that can recover lost energy[5].

Partial Adiabatic Logic (PAL) circuits have emerged as a promising solution, offering a balance between performance and power consumption[6]. Powered by complementary four-phase power clocks, these circuits address the growing power challenges in modern electronics, especially in nanoscale CMOS technology, where traditional low-power techniques face limitations due to technology scaling These circuits represent an innovative approach among various energy-efficient design techniques aimed at reducing significant power dissipation. This approach leverages energy recovery mechanisms, allowing for substantial power savings in critical components such as adders, multiplexers, and filters. PAL techniques specifically target the reduction of power dissipation in digital circuits, particularly for low-power applications. While traditional logic circuits waste power through dynamic charging and discharging of capacitances, along with static power losses, adiabatic logic techniques seek to recover and reuse this energy, thereby minimizing overall power loss[7]. One of the main features of adiabatic logic is that it can operate efficiently at a frequency less than 1 GHz. Thus, adiabatic logic can be used to design Low Power devices which operate at low frequencies.

Reviewing PAL style will provide valuable insights into the fundamentals of Adiabatic Logic, including key techniques like ECRL, PFAL, and DCPAL[8]. This review aims to explore the principles, advancements, and challenges associated with partial adiabatic logic techniques, with a focus on their application in low-power VLSI circuits. We provide a comprehensive analysis of the key methods, the impact of technology scaling, and the potential of partial adiabatic logic in addressing the ever-growing demands for energy-efficient digital systems. By highlighting recent developments and future directions, this review seeks to contribute to

the understanding and adoption of partial adiabatic logic in the design of power-efficient VLSI circuits. This review will assess their effectiveness in various circuit designs, compare power savings with conventional CMOS logic, identify potential limitations, and explore new strategies for integrating PAL into modern semiconductor processes to enhance compatibility with existing technologies[9]. While the potential of adiabatic logic to reduce power dissipation is well recognized, understanding the underlying principles and methodologies is essential for its effective application. Adiabatic logic is based on key concepts such as energy recovery, slow switching, and reversible computation, which distinguish it from conventional CMOS circuits.

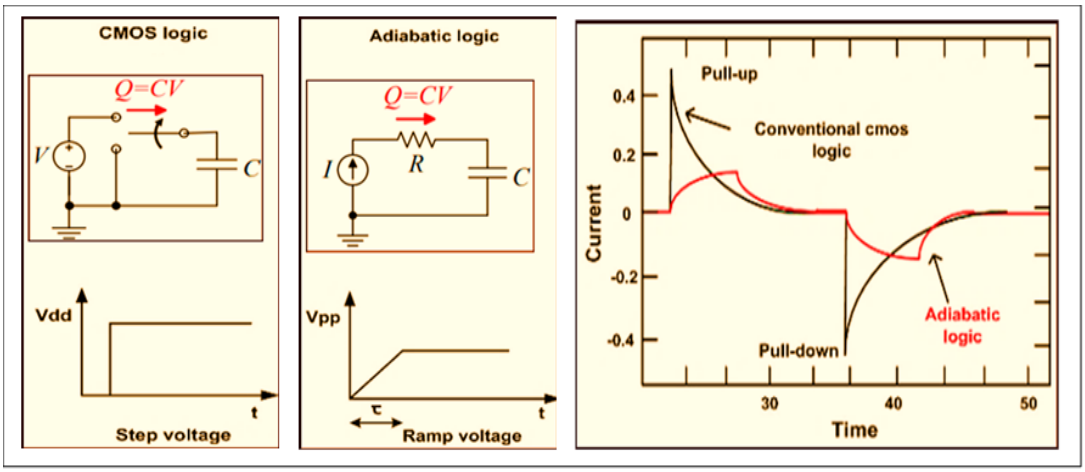
In next section, we explore the fundamental principles behind adiabatic logic and the methodology used to design these circuits. By examining these principles in detail, we can understand how adiabatic logic operates in a practical setting and the benefits it offers in terms of energy efficiency. Further, the realization of adiabatic logic circuits and the implementation of an adiabatic power clock is discussed. This involves not only theoretical understanding but also the engineering of circuits that can efficiently implement the principles of energy recovery and low-power switching. Specifically, a crucial aspect of adiabatic logic realization is the implementation of an adiabatic power clock, which plays a vital role in managing the gradual transition of voltage and facilitating energy recovery.

2. ADIABATIC LOGIC PRINCIPLES AND METHODOLOGY

Adiabatic, in its original thermodynamic sense, describes a process where there's no exchange of energy with the surroundings, thus no energy loss through dissipation[10]. However, in microelectronics, charge transfer between circuit nodes is indeed considered a process. Here are the fundamental guidelines for adiabatic circuits to follow[11], [12]:

1. Avoid turning on a transistor if there's a non-zero voltage across drain and source ports.
2. Avoid abrupt changes in voltage across any activated transistor.

Adhering to these principles imposes the use of adiabatic switching. Traditional CMOS circuits establish either a logic '1' or '0' by charging the load capacitor to the supply voltage V_{dd} and then discharging it to ground, respectively[13]. Consequently, with each charge-discharge cycle, an energy equivalent to $CV_{dd}{}^2$ is expended. In contrast to this, adiabatic circuit is designed with reversible logic in such a way that it recovers and reuses the energy stored in load capacitors instead of being discharged to ground and get wasted. Adiabatic strategy uses slow operational speed and switching of transistors under certain circumstances. When a steady current power source (such as an AC power clock, pulsed power supply, clock generator, resonance LC oscillator, etc.) is deployed in place of an unvarying voltage (DC) power-source, a slow change can be achieved[14]. A constant voltage scaling in CMOS circuit as shown in Fig. 1(a) brings out step voltage causing maximum power dissipation whereas a constant charging current power supply I(t) in adiabatic circuit shown in Fig. 1(b) doesn't change suddenly from 0 to V_{dd} or vice -versa, and brings out a linear voltage ramp. In adiabatic circuits, the utilization of four-phase trapezoidal power clock line is necessitated to achieve the inbuilt pipelining of the electronic devices and "reversible logic" is applied to moderate the peak current flow through the circuit thus leading to immense low power dissi-



(a) (b) (c)

Fig. 1. Equivalent RC models depicting the (a) step voltage of CMOS logic (b) the ramped step voltage of adiabatic logic (c) Graph of peak supply current in (a) and (b) under the identical parameters and condition [19]

pation that highly depends upon power clock and parameter variations[15].

In the context of the time interval T, when a consistent current supply provides a charge of Q($= CV_{dd}$) the measure of dissipated energy in the channel with a resistance, R, can be stated by a subsequent equation[16]:

$$E_{dissipated} = I^2RT = \left(\frac{CV_{dd}}{T}\right)^2 RT = \left(\frac{RC}{T}\right) CV_{dd}^2 \qquad (1)$$

As per eq (1), it can be observed that the adiabatic switching dispersion of power exhibits an asymptotic proportionality to the reciprocal of the charging time constant (T). If T is made satisfactorily larger than RC (T>>2RC), such that $E_{dissipated}$ will become nearly zero which is ideally required[17]. Thus, a part of energy stored in capacitor can be recovered back by reversing the direction of current source which allows charge to route back to input power supply to used again. This process is called as Adiabatic Switching[18].

Fig. 1(c) compares peak current traces of conventional CMOS logic and adiabatic logic using their equivalent RC models [19]. The CMOS graph shows a sharp current surge (black line) contrasting with the gradual rise in supply current peak (red line). In contrast, adiabatic logic exhibits lower peak currents than CMOS. As power dissipation correlates with voltage and instantaneous current, the overall current flow in adiabatic circuits is lower, leading to substantially reduced power dissipation compared to conventional CMOS logic[20].

During the evaluation period, the clock signal (Clk) rises while its complement ($Clk\bar{}$) falls. If the output is low and the P-type MOS transistor is activated, the capacitor charges, leading to a high output, as shown in Fig. 9(b). Conversely, during the holding phase, Clk falls while $Clk\bar{}$ rises. When the N-type MOS transistor activates and the output goes high, the capacitor

discharges, resulting in a low output logic. The complementary clock signals help mitigate leakage effects, reducing delay and thereby lowering the Power Delay Product (PDP), a critical metric for assessing digital circuit efficiency[21], [22].

2.1 Realization of Adiabatic logic circuit

To enhance the vitality competence of logic circuits, the circuit design and operating standards must be modified when the requirement arises[23]. The steps listed below must be performed in order to realize a basic CMOS gate into an adiabatic logic gate:

1. Replace all pMOS and nMOS components with T-gates (Transmission Gates) in the circuits for the P-U- N/W and P-D- N/W.
2. The extended P-U- N/W is utilized for the purpose of energizing the actual output.
3. Enhanced PDN pushes complementary output to true output.
4. The load capacitance in the modified circuit is charged and discharged using both networks.
5. To enable adiabatic operation, swop DC V_{dd} with a pulsed power AC source with variable voltage and constant current.

The adiabatic logic circuit uses both PU N/W and PD N/W for charging and releasing the output node capacitance C_L, ensuring that the energy saved is not lost [24]. At the conclusion of each cycle the power supply may be extracted at the output node[25].

2.2 Adiabatic Power Clock

An integral part of the adiabatic operating idea is the power clock, which undergoes significant modifications in the adiabatic design[26]. A trapezoidal or sinusoidal voltage source is typically used as the constant-current source. Here, a power source and a clock are combined to form the power clock which implies that it has different voltage and frequency levels and hence, known as "power clock". It enables bidirectional flow of charge between the load and the power-clock, thereby recycling specific extents of energy retained from node capacitors back into the power source, leading to reduced power consumption[27].

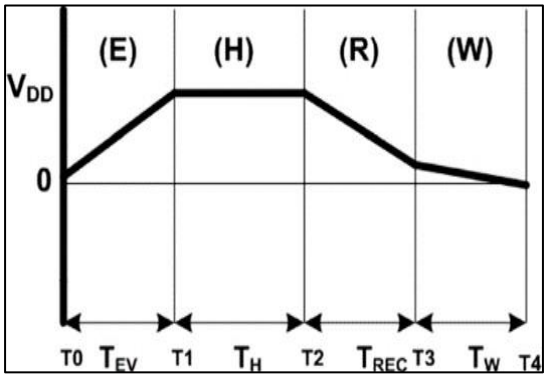


Fig. 2. A cycle of trapezoidal power clock

As illustrated in Fig. 2., the configuration of PC facilitates the functioning of adiabatic circuits through four distinct phases each with a phase deviation of one-fourth of a complete period[28]:

1. Evaluation phase, during which PC rises from 0 V to its peak voltage (V_{dd});
2. Hold phase, where outputs are kept stable in hold state to enable the evaluation of input for subsequent stage pipelining and PC remains high during this phase.;
3. Recovery phase, as PC descends from its peak voltage to 0 V, permitting the recovery of charge from load capacitor at output node; and
4. Wait phase, characterized by PC resting at 0 V, facilitating synchronization across stages. Finally, the capacitor is fully discharged during the waiting time[29].

By carefully controlling the evaluation, stability, energy recovery, and timing of the circuit's operation, power clocks with these phases help reduce power consumption in digital systems where energy efficiency is a key concern[30]. The following section presents a comprehensive survey of partial adiabatic logic techniques, highlighting their principles, notable implementations, and applications in low-power VLSI design. This review aims to contextualize the challenges identified and identify opportunities for further optimization.

3. LITERATURE SURVEY OF ADIABATIC LOGIC FAMILIES

The adiabatic power clock, as discussed, is a critical component in the realization of adiabatic logic circuits, enabling the gradual voltage transitions necessary for energy recovery and minimal power dissipation. Its design and implementation significantly influence the overall performance and efficiency of adiabatic circuits. While understanding the underlying principles and methodologies is essential, it is equally important to examine how these concepts have been applied in practice and how they have evolved over time.

In the literature, various studies have explored different approaches to designing and optimizing adiabatic power clocks, as well as the broader application of adiabatic logic circuits in low-power VLSI systems. Researchers have proposed a range of techniques to enhance energy efficiency, address limitations, and improve the scalability of adiabatic logic. A comprehensive review of these studies provides valuable insights into the progress made in the field and identifies the challenges that still need to be addressed.

Therefore, in this section, we present a Literature Survey that highlights the key research efforts, trends, and advancements in the field of adiabatic logic. This survey serves as a foundation for understanding the current state of the art and sets the stage for discussing potential future directions in low-power VLSI design using adiabatic logic.

Based on the extent of energy recovery, adiabatic logic is broadly classified into Partial Adiabatic Logic (PAL) and Fully Adiabatic Logic (FAL), each with unique advantages, challenges, and applications. Numerous researchers have proposed and refined both partial and fully adiabatic logic approaches to improve energy efficiency.

While FAL circuits aim for zero un-adiabatic power dissipation, PAL circuits inherently involve faster operation with some level of such dissipation[31], [32].

1. Partial-adiabatic circuits: In PAL circuits, some amount of heat is dissipated by the transfer of some charge to the ground. Therefore, only a portion of the energy may be recovered. Partial adiabatic circuits feature a simple architecture with few adiabatic losses in certain operational regions and exits. Efficient Charge Recovery Logic (ECRL), Positive Feedback Adiabatic Logic (PFAL), 2N-2N2P and 2N-2N Logic and Diode Connected, DC- biased Positive Feedback Adiabatic Logic (DCDB-PFAL), Differential Cascode, and Pre- resolved Adiabatic Logic (DC-PAL), Diode Free Adiabatic Logic (DFAL), and Modified Quasi-Static Energy Recovery Logic (MQSERL) are some of the commonly used partial adiabatic logic techniques[33], [34].

2. Fully Adiabatic circuits: In FAL circuits, all charges present on the load capacitance are recuperated and redirected towards the power source, thus rendering them slower and more intricate than PAL circuits. There are several challenges associated with the operational speed and input-fed power-clock synchronization in FAL circuits. Few FAL families are Pass Transistor Adiabatic Logic (PTAL), Split-Level Charge Recovery Logic (SCRL)[35] and Two-Phase Adiabatic Static Clocked Logic (2PASCL)[36], [37].

PAL circuits offer a balanced approach, while FAL circuits provide the highest level of energy efficiency as at the expense of speed and increased design complexity[38]. The choice between these approaches' hinges on the specific requirements of the application and desired trade-offs between power consumption and performance. Partial adiabatic logic has been extensively studied due to its practicality and ability to balance energy recovery and design complexity.

In the existing literature, some of the prevailing variants of PAL circuits such as ECRL, 2N-2N2P, PFAL, DCDB-PFAL, DC-PAL, DFAL, and MQSERL have been proposed to improve the power dissipation of VLSI electronic systems for low-power applications[39]. While these adiabatic logic circuits offer energy-saving potential, they also arise challenges related to complexity, speed, and practical implementation. Adiabatic circuits like ECRL, 2N-2N2P, PFAL and DCDB-PFAL function using a single power clock signal, whereas DCPAL, DFAL and MQSERL employ two power clock signals with a pre-resolving phase, followed by wait, evaluation, hold, and recovery phases[40].

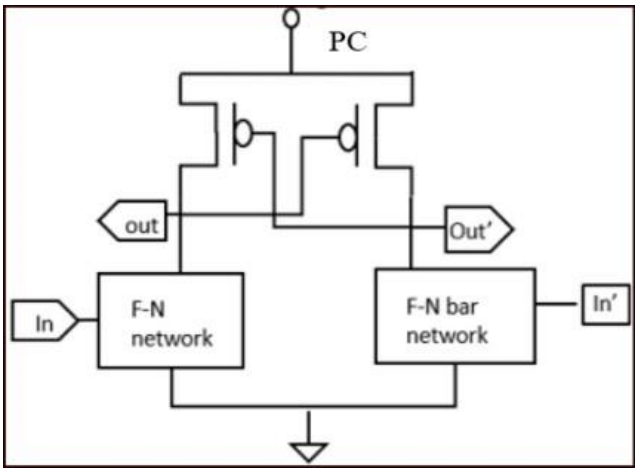
This paper offers an extensive examination of afore-mentioned PAL techniques documented in existing literature. The main aim is to implement architecture and conduct simulations for circuits based on PAL and evaluate their performance in terms of power dissipation, propagation delay, and power savings. Among the PAL families outlined in literature, the following have been subjected to implementation, simulation and analysis[41].

3.1 Efficient Charge Recovery Logic (ECRL)

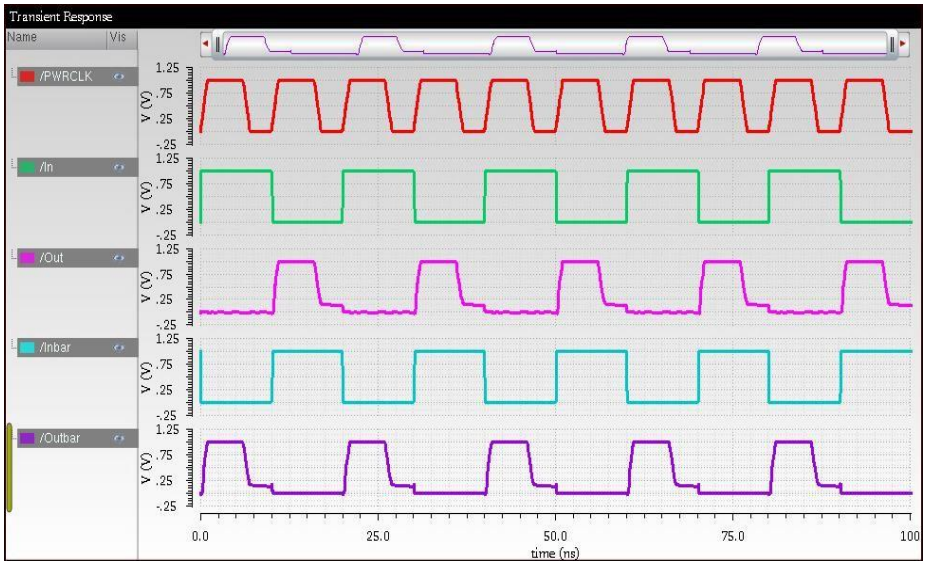
Originally proposed by Dickinson and Denker in 1995, ECRL is a widely studied partial adiabatic logic family. ECRL is aimed at enhancing the performance of adiabatic logic circuits efficiently. The circuit depicted in Fig. 3(a) comprises a pair of pull-down NMOS devices to evaluate functions and a pair of cross-coupled pull-up PMOS transistors to hold the state [42]. It is energized by an AC power source with four-phase power clock signal[43].

Complete recovery of Input is not possible with PMOS transistors, so it is still a PAL technique. The reason behind the provision of dual outputs, specifically out and out', is to let the continual functioning of the pwr_clk. This, in turn, allows for the autonomous driving of a uniform load capacitance, irrespective of the input signal[44].

Due to the cross coupled PMOS, full output swing is found in both precharge and recovery phase as the output of one inverter influences an outcome of the corresponding inverter, and vice versa. But the circuit exhibit coupling effects and non-adiabatic losses during the pre-charge and recuperate stages, which can be accredited to the brink voltage of the P-type MOS transistors[45].



(a)



(b)

Fig. 3(a) Schematic of Conventional ECRL (b) Output waveform of ECRL Inverter

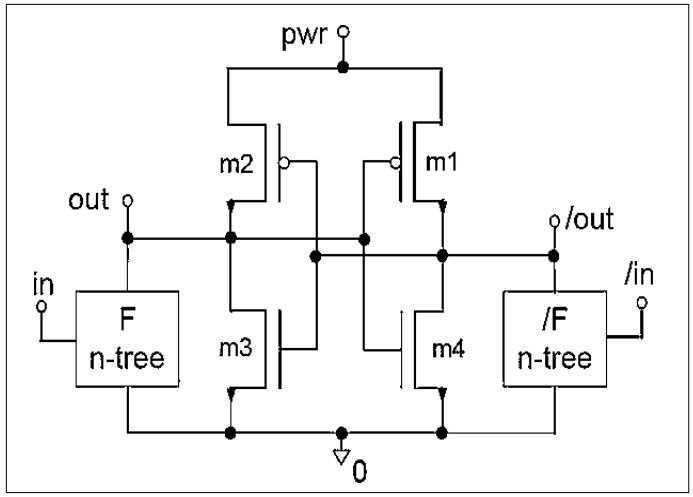
Fig. 3(b) depicts the output response for an ECRL inverter. The variables In and Inbar represent pulse inputs. The two outputs Out and Outbar exhibit an inversion of the two inputs when pwr_clk (pc) is high. Consequently, if input In is (1), it is necessary for the Inbar to be (0). In this scenario, the NMOS transistor NM1 is activated ceasing NMOS transistor NM0, and connects Out to the ground offering a zero output that is the inverted equivalent of the input In (1). The activation of Out occurs upon its connection to PMOS (PM0), whereby the capacitor at Outbar is charged through the current flowing from trapezoidal pwr_clk (pc) to Out, resulting in high output that is the inverse of the signal Inbar[46]. Studies have shown that ECRL circuits achieve significant power savings in comparison to static CMOS, particularly in low-frequency applications. However, parasitic losses and incomplete recovery remain key limitations.

3.2 2N-2N-2P logic

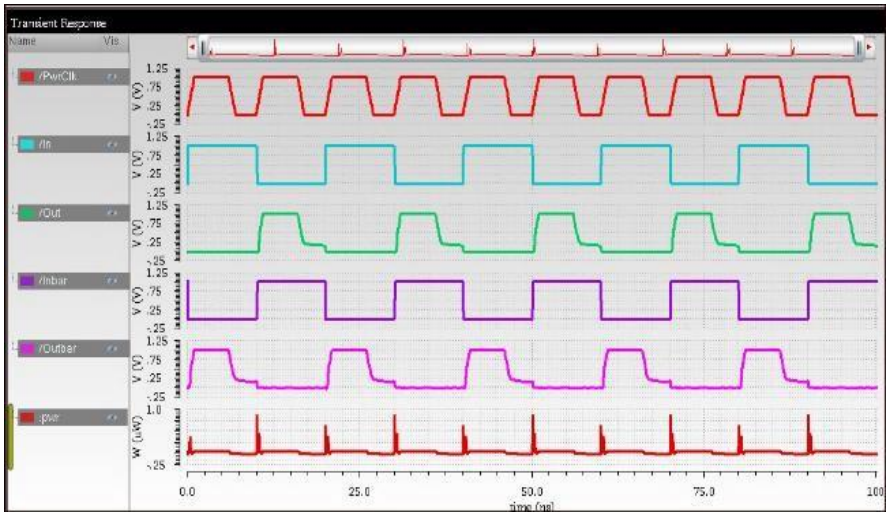
Various studies have investigated the 2N-2N2P logic, which uses complementary pass-transistor structures for energy-efficient operation. To mitigate the coupling impact, ECRL logic was modified to 2N-2N-2P logic. Following is a general illustration of 2N-2N-2P logic as shown in Fig. 4(a): Instead of only two NMOS as in the ECRL logic family, the 2N-2N-2P logic has a cross-coupled latch consisting of two PMOS(m1-m2) and two NMOS (m3- m4) Although the N-functional block is in parallel with the NMOS of the latch and thus, takes up more space. One advantage of utilizing 2N-2N2P instead of ECRL is that the non-floating output is provided for a considerable duration of the recovery period due to the implementation of cross-coupled NMOS switch configuration as can be seen in the waveform Outbar and Out from the Fig. 4(b) that describes the 2N-2N-2P inverter output waveform[47].

Two cross-coupled P-type MOS transistors are utilized by the 2N-2N-2P logic for both precharge and recovery, hence the following Eq (2) describes its energy loss per cycle[48]:

$$E_{2N\text{-}2N2P} = 2\left(\frac{R_P C_L}{T}\right) C_L V_{dd}^2 + C_L V_{TP}^2 \qquad (2)$$



(a)



(b)

Fig. 4(a) 2n2n2p General Schematic (b) Output response of 2N-2N-2P inverter

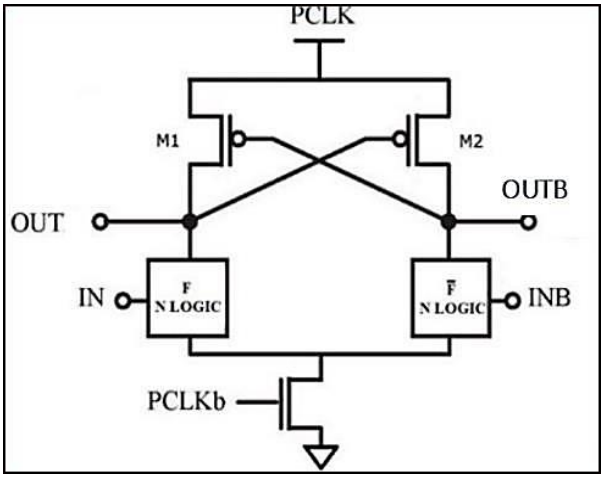
The first component in the above equation reflects the complete adiabatic loss, which can be decreased by minimizing the operating frequency, while the second term indicates the non-adiabatic energy loss, which is independent of the operation frequency[49]. This method achieves partial energy recovery while offering a compact design. However, its application is limited by the increased delay in high-speed circuits.

3.3 Differential Cascode, and Pre-resolved Adiabatic Logic (DC-PAL)

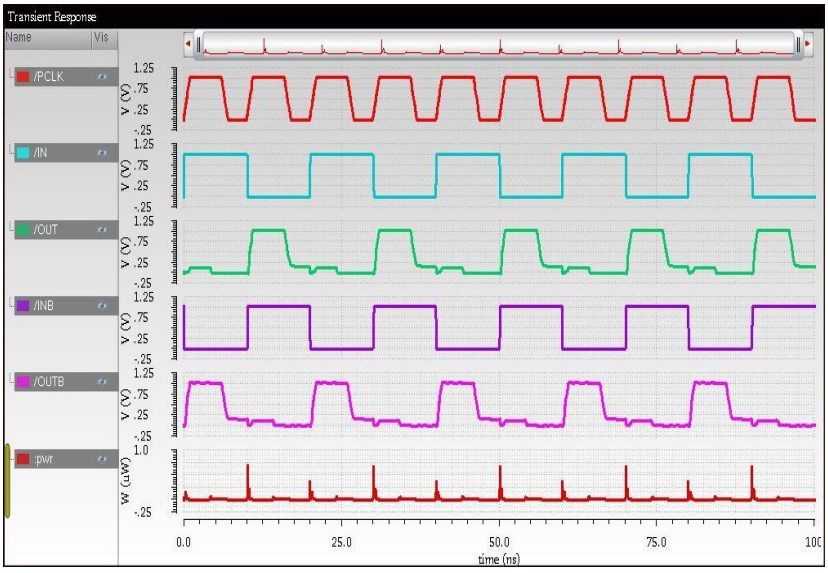
DCPAL (Differential Cascode and Pre-resolved Adiabatic Logic) is a type of adiabatic logic designed to improve energy efficiency while reducing power consumption, especially in low-power VLSI applications. It combines differential signaling and cascode transistors with pre-resolved logic, enabling partial energy recovery during logic transitions. DCPAL, an acronym for Differential Cascode and Pre-resolved Adiabatic Logic, refers to a meticulously structured dual rail logic system. The architecture of DCPAL, as depicted in Fig.5(a), bears resemblance to that of ECRL. Research on DCPAL has also focused on improving clocking schemes to reduce power loss during logic transitions. Newer methods have been proposed for dynamic clocking, which further enhances the energy recovery and overall performance of DCPAL circuits [50]. However, an additional footer transistor is incorporated in DCPAL circuitry and extra power clock (PCLKb) at its gate terminal. The aforementioned complementary power clocks PCLK and PCLKb are used the purpose of pre-resolving the inputs.

DCPAL offers enhanced functionality, accommodating larger fan-in and boasting high energy efficiency as shown in Fig. 5(b) its output waveform. This diode-free, dual-rail logic employs a four-phase power clock for its adiabatic pipeline operation. With its streamlined design featuring a differential cascode structure and fewer transistors, DCPAL achieves reduced latency. Its pre-resolving capability for complementary inputs contributes to a significant decrease in switched capacitance, leading to improved power efficiency and silicon area utilization. Additionally, DCPAL ensures reduced leakage paths and delivers glitch-free

output with minimized switching transients. Research has shown that DCPAL provides better energy recovery than traditional CMOS logic and other partial adiabatic families like ECRL or PFAL. Studies highlight that DCPAL achieves a balance between energy efficiency and design complexity, making it suitable for low-power and battery-operated devices[51].



(a)



(b)

Fig. 5(a) DCPAL Circuit (b) its output waveform

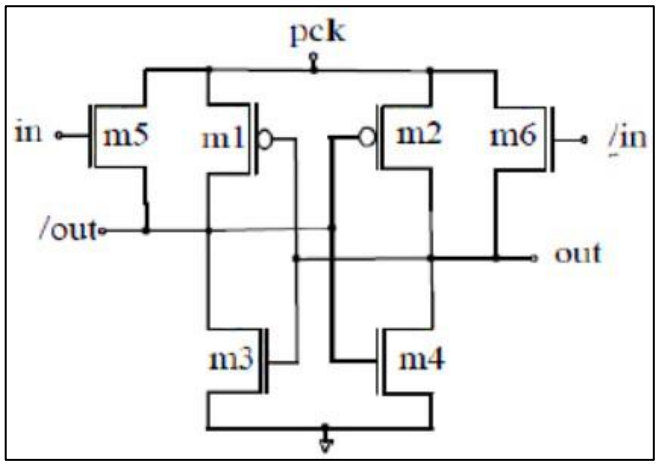
3.4 Positive-Feedback Adiabatic Logic (PFAL)

PFAL, introduced by Vetuli in 1996, builds upon the principles of ECRL by incorporating a feedback mechanism to maintain the output state. PFAL is partially energy recovery logic since

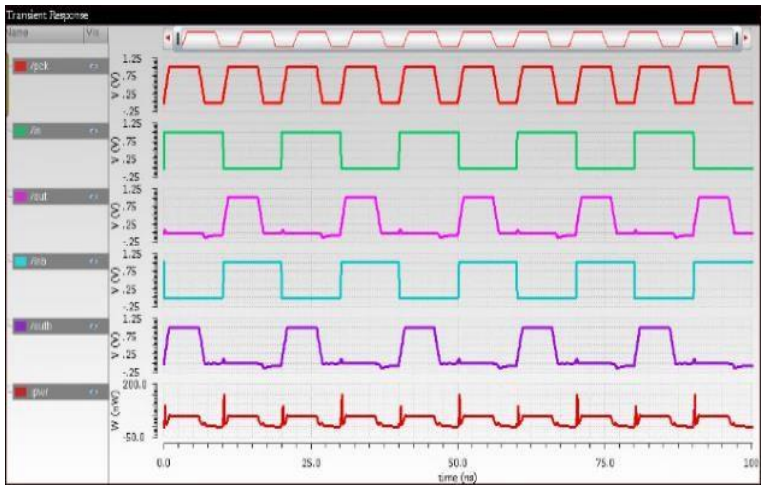
it consumes a remarkably very low power in comparison to other adiabatic logic families[52].

One notable distinction between ECRL and PMOS pertains to the alignment of the latch. ECRL specifically comprises two PMOS and two NMOS whereas PFAL, comprises the same two PMOS and two NMOS, along with the functional nmos units parallel with the upper two PMOS and form the transmission gates. Consequently, when the capacitor is charged, the equivalent R is lesser [53].

As shown in Fig. 6(a), It is a dual rail circuit with some energy recovery. The PFAL circuit's logic function determines whether the output (out) remains at a low voltage level or changes on the rising edge of the power clock signal from gnd to V_{dd} [54]. In PFAL, Inputs is given on the one side and outputs are taken from the opposite side. A logical value of zero and V_{dd} is denoted by the variables "out" and "/out" up until the power clock hits V_{dd}.



(a)



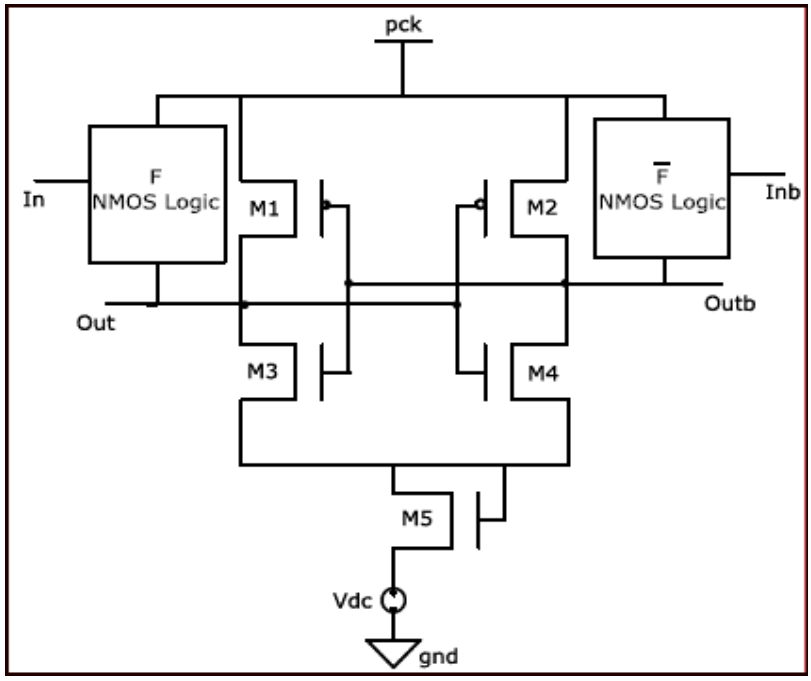
(b)

Fig. 6 (a) PFAL Logic circuit (b) PFAL Inverter Output response

3.5 Diode connected DC biased Positive Feedback Adiabatic Logic (DC-DB PFAL)

In PFAL, leakage currents leak from the voltage source to ground during evaluation, hold, and recovery, causing dissipation of charge that cannot be retrieved back. Recent studies have highlighted the energy recovery capabilities of DCDB-PFAL in comparison to other partial adiabatic logic families such as ECRL and PFAL. Simulations have shown that DCDB-PFAL can achieve significant reductions in power dissipation for low-frequency circuits. The circuit illustrated in Fig. 7(a) is an enhanced version of PFAL, referred to as DCDB-PFAL ("Diode-connected, DC-biased" Positive-Feedback Adiabatic Logic) [56].

The generalized diagram of DCDB-PFAL is a reminiscent of PFAL logic with a latch comprising two PMOS and two NMOS transistors. NMOS logic blocks are linked in parallel with the PMOS transistors, forming transmission gates similar to PFAL. Notably, the pull-down mechanism deviates by incorporating an NMOS diode and DC voltage source between the pull-down NMOS transistors and ground. This setup aims to regulate discharge paths, reducing internal node discharge rate. Researchers have focused on optimizing the diode-connected transistor structure and DC biasing to further enhance the performance of DCDB-PFAL. Techniques to minimize parasitic effects and improve energy recovery during the switching process have been explored [56].



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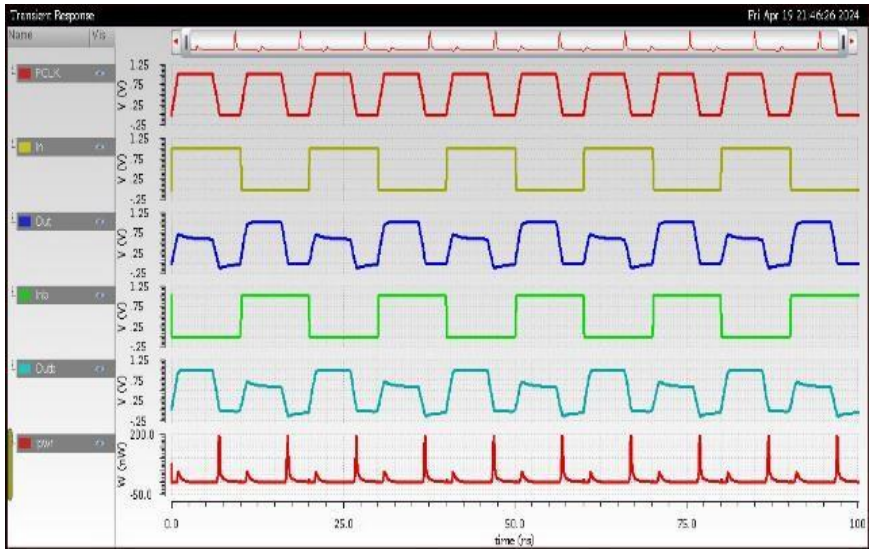


(b)

Fig. 7 (a) DCDB-PFAL circuit (b) its Output waveform

Additionally, a positive DC voltage source is introduced between the diode and ground to enhance level shifting, lowering gate-to-source voltage across output transistors and reducing gate and leakage currents. The magnitude of this voltage source ranges from 0.3 V to 0.7 V, with subsequent simulations conducted. It can be seen that with the use of an NMOS diode and with increasing the DC voltage both the voltage difference and the current start reducing. And thus, a further reduction in power dissipation is achieved. The lowest power is attained at 0.7 DC voltage and after that it starts increasing. The circuit attains low-power operation because a low DC Source is connected to the circuit in series. Thus, the DCDB-PFAL provides lower power dissipation as compared to conventional PFAL logic circuit. DCDB-PFAL improves energy recovery, reduces idle power dissipation, and simplifies clocking compared to fully adiabatic circuits. Its applications in low-power arithmetic circuits, memory designs, and battery-powered devices highlight its potential for energy-efficient VLSI systems. However, challenges related to partial energy recovery and design complexity remain, requiring further optimization for high-speed applications and enhanced efficiency.

3.6 Diode Free Adiabatic Logic (DFAL)

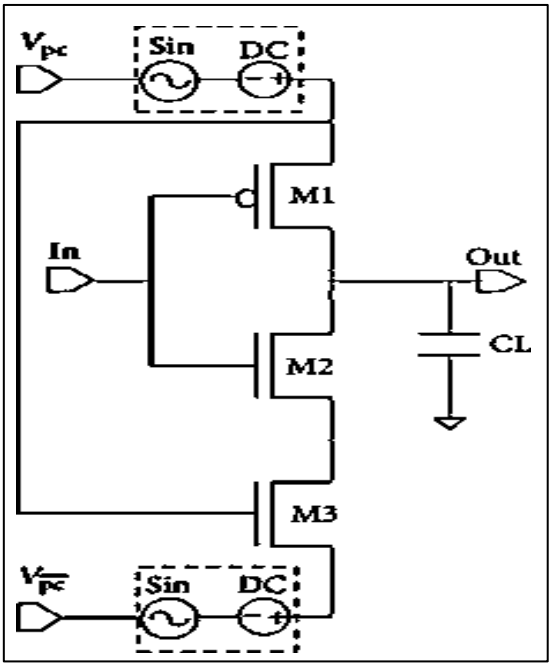
Diode-Free Adiabatic Logic (DFAL) is a variant of adiabatic logic that eliminates the need for diodes, which are traditionally used in various adiabatic logic families to recover energy. By removing the diodes, DFAL aims to reduce the complexity and improve the efficiency of energy recovery in low-power circuits. This logic family is particularly appealing for low-power VLSI designs, as it minimizes power dissipation while achieving partial energy recovery during logic transitions.

The DFAL circuit bears a resemblance to a static CMOS circuit, perhaps operating in an adiabatic mode. The pull-down N/W next to M2 confronts a replacement of the diode with an NMOS transistor (M3). The transistor M3 is controlled by the voltage-controlled power clock

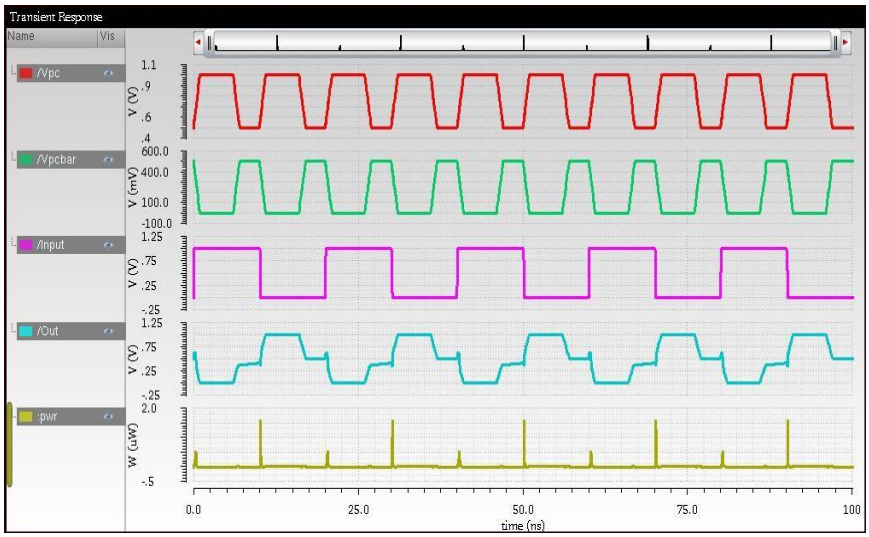
(V_{PC}) to facilitate its ON/OFF switching. DFAL has been widely explored in low-power arithmetic circuits, such as adders and multipliers, as well as memory systems where its low power dissipation during idle periods and energy recovery during transitions can lead to substantial power savings[57]. The circuit layout and generated output waveform used to assess the performance of a DFAL-based inverter are illustrated in Fig. 8(a). The absence of a diode in the powering or dispensing routes of this logic circuit renders it an attractive option.

The utilization of V_{PC} and $V_{\overline{PC}}$ is employed in the implementation of the split-level sinusoidal power clock[58]. The 1st clock is operating in synchronization, while the 2nd clock is in a state of desynchronization. The voltage at which V_{PC} exceeds that of $V_{\overline{PC}}$ by a fraction of $V_{PC}/2$, there occurs a reduction in the voltage divergence between the electrodes. As a result, the aforementioned action leads to a decrease in the dissipation of power. Recent studies have compared DFAL with other partial adiabatic logic families, such as PFAL and ECRL, showing that DFAL strikes a balance between energy efficiency, design complexity, and scalability.

The primary source of power dispersion in adiabatic circuits, as described, takes place during the discharge period, specifically at the MOS diodes. This is attributed to the threshold potential drop, which is a non-adiabatic loss. However, in the case of the DFAL circuit, the power dispersal is primarily due to the adiabatic loss resulting from the ON resistance of the MOS transistor's (M3) channel. This M3 ON resistance consumes far less power than the threshold potential, which lessens through diodes. The utilization of M3 also serves the purpose of recycling electrical charge from the resultant node, thereby enabling more recuperation of adiabatic losses.



(a)



(b)

Fig. 8(a) Schematic of DFAL Inverter (b) DFAL Output waveform

Fig. 8(b) illustrates the output response of DFAL inverter. This no-diode energy recovery circuit is subject to irreversibility, which precludes the complete recovery or elimination of losses and dispersal of power as a consequence, using MOS transistor M3 dramatically decreases power dispersal in contrast to diode-based energy recovering circuits. The DFAL inverter exhibits a superior energy efficiency of more than 60% up to 100 MHz when compared to conventional CMOS devices. Researchers have proposed methods to further improve DFAL's clocking schemes, optimizing them to reduce switching losses and enhance overall efficiency. This has led to advancements in DFAL's integration into modern low-power, high-performance systems.

3.7 Modified Quasi-Static Energy Recovery Logic (MQSERL)

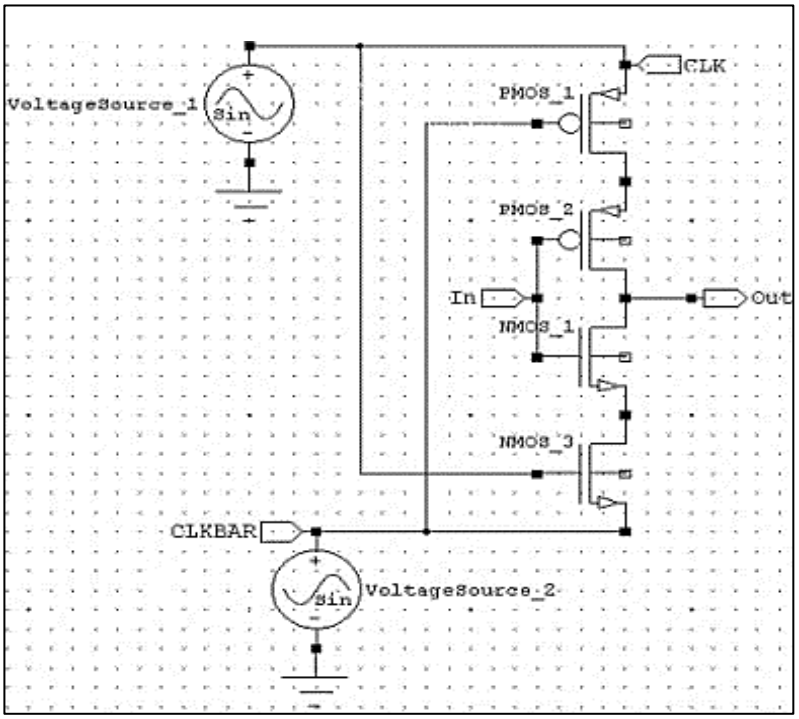
Adiabatic logic families, such as QSERL, have garnered attention due to their ability to recover energy during logic transitions, significantly reducing the energy dissipated in switching operations compared to traditional CMOS circuits. However, the original QSERL design has certain limitations, including slower switching speeds, larger circuit area, and limited energy recovery efficiency.

QSERL is a technique that utilizes two sinusoidal power clocks that are complementary to each other to circumvent the drawbacks of dynamic adiabatic circuits. It exhibits static CMOS logic characteristics that result in reduced switching activity of nodes and it's not necessary for circuit nodes to undergo charging or discharging during each clock cycle, thereby reducing energy dissipation. There are two phases: hold and as a consequence of the alternating hold phases, the QSERL final output is found in a floating state, which leads to Insufficient resilience or durability[59]. MQSERL was developed as an enhancement to QSERL, addressing these drawbacks while maintaining the core advantage of partial energy recovery.

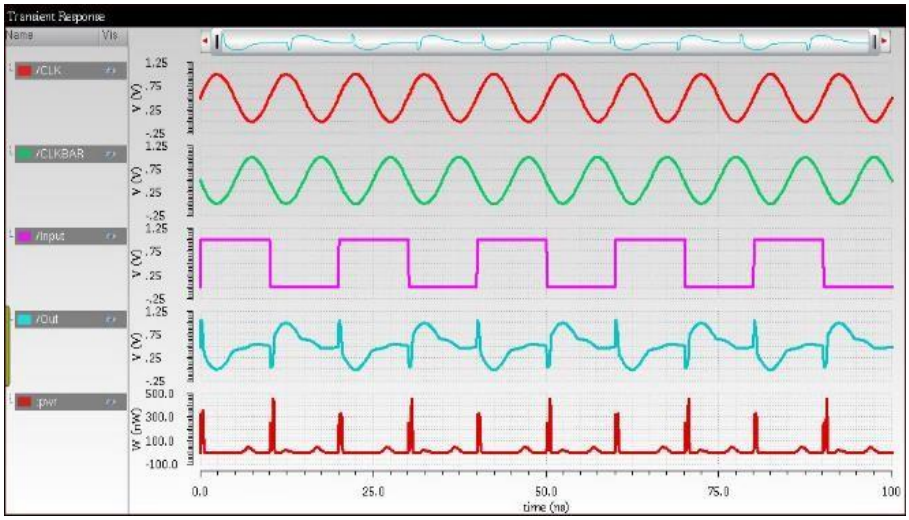
The goal of MQSERL is to provide a more efficient and practical solution for low-power and high-performance applications, where both energy recovery and speed are critical. So, the new Modified Quasi-Static Energy Recovery Logic (MQSERL) circuit was specially designed to address the drawbacks of QSERL. This circuit preserves all positive attributes of QSERL and can serve as a suitable replacement for CMOS logic. MQSERL has been applied to arithmetic circuits, such as multipliers and adders, where energy efficiency is crucial. These studies have highlighted MQSERL's potential for reducing energy dissipation in circuits that perform frequent switching during operations[60].

Recent research has focused on optimizing the PDP of MQSERL circuits. Studies have shown that MQSERL can achieve a better balance between power efficiency and speed when compared to traditional CMOS logic and other adiabatic logic families. By fine-tuning the switching parameters, several studies have demonstrated that MQSERL can be adapted for both low-power and high-speed applications, making it a versatile logic family.

Fig. 9(a) illustrates an enhanced quasi-static adiabatic logic design featuring a P-type MOS transistor at the top, linked to a clock signal, and an N-type MOS transistor at the bottom, connected to a clock signal that is 180° out of phase. The P-type transistor controls the charging path, while the N-type regulates the discharging path.



(a)



(b)

Fig. 9(a) Design of M-QSERL inverter (b) Simulation response of M-QSERL

This architecture simplifies circuit complexity in terms of wiring and design compared to QSERL. The two clock signals exhibit complementary sinusoidal waveforms, minimizing energy dissipation. The load capacitance gradually charges and discharges, operating in two main periods: evaluation and holding[61]. Researchers have explored different techniques to balance energy recovery and speed in MQSERL. By fine-tuning the switching parameters, several studies have demonstrated that MQSERL can be adapted for both low-power and high-speed applications, making it a versatile logic family.

4. CIRCUIT SIMULATION AND RESULTS

Having reviewed the existing advancements and challenges in the realm of adiabatic logic circuits, particularly focusing on the PAL circuits, it becomes clear that the practical application of these logic families hinges on optimizing both energy recovery efficiency and switching performance in real-world circuit designs. Although numerous improvements have been proposed in the literature, the actual performance of these circuits in terms of power consumption, speed, and area efficiency must be validated through practical simulation to determine their real-world performance in terms of power consumption, speed, area, and overall system efficiency.

Building on the insights gained from the literature and to further explore the practical implications of these techniques, this section presents the simulation methodology, the circuit models used, and present the detailed results obtained for various configurations. The performance of each adiabatic logic technique will be assessed and compared with traditional CMOS inverter configuration across key parameters such as power dissipation, delay, and power savings under typical operating conditions to provide insights into their potential for

low-power, high-performance VLSI applications. Through these simulations, we aim to verify the theoretical advantages highlighted in the literature and provide a deeper understanding of the practical trade-offs involved in using PAL circuits for low-power applications.

In order to analyze the effectiveness of PAL circuits over CMOS logic, inverters have been simulated using existing adiabatic logic families[62]. Since adiabatic style circuits are influenced by fluctuations in factors such as voltage and frequency, to compare adiabatic logic-based inverters with a CMOS inverter, several key aspects such as power dissipation at different frequencies and different voltage supply and propagation delay have been measured with reference to [55]-[59]. Adiabatic logic-based inverters exhibit different power dissipation levels depending on the various simulation parameters. The implementation of CMOS & Adiabatic Logic designs for inverters is done using Cadence Virtuoso EDA tool at 90nm technology node at room temperature of 27o with parameters taking as mentioned in Table I[67].

5. COMPARISON OF PERFORMANCE METRICS OF PAL TECHNIQUES AGAINST TRADITIONAL CMOS

The simulation results for the various Partial Adiabatic Logic (PAL) techniques, including MQSERL, DCPAL, and PFAL, have demonstrated promising improvements in power efficiency, energy recovery, and delay compared to conventional digital circuits. These results underscore the potential of adiabatic logic in reducing dynamic power dissipation and achieving low-power operation in digital circuits. However, to assess the real-world viability of these techniques, it is essential to compare their performance with the dominant logic family in current VLSI design: traditional CMOS.

While CMOS technology remains the backbone of modern digital circuits due to its low cost, scalability, and well-established design practices, the growing demand for energy-efficient systems in areas such as mobile devices, IoT, and high-performance computing has driven the exploration of alternative logic families, such as adiabatic logic. Therefore, comparing the simulation results of PAL techniques with CMOS is crucial for understanding their relative strengths and weaknesses in practical applications.

In this section, we will perform a comparative analysis of Partial Adiabatic Logic (PAL) techniques with traditional CMOS circuits. This comparison will focus on key performance metrics such as power dissipation, number of transistors used, delay and power savings which are critical factors in determining the feasibility of adopting adiabatic logic for low-power, high-performance applications. Also, effect of variation in frequency of power clock of adiabatic circuit on the power dissipation of the circuit is analysed as it is one of the important reliability parameters of the adiabatic circuit on which the power consumption depends directly.

Table II compares different adiabatic inverters based on their number of transistors, power dissipation at different supply voltages. Each logic family has different power dissipation characteristics at different voltage levels[68]. It can be observed that DC-DB PFAL and DCPAL exhibit relatively low power dissipation of 12.40nW and 5.778nW across all voltage levels whereas while CMOS has the highest power dissipation of 147.8uW at 3V, signifying

TABLE I DESIGN PARAMETERS FOR ANALYSIS

Simulation parameters	Values
Parameters to be measured	Power Dissipation and Propagation Delay
Technology	90nm
Input Voltage	1V
Input frequency	50 Hz
PC Voltage (Vdd)	1V,2V,3V
PC Frequency	100MHz, 200MHz, 500MHz
Transition time	100ns
Rise time of PC	1ns
Fall time of PC	1ns

TABLE II COMPARISON OF POWER AND DELAY OF DIFFERENT ADIABATIC INVERTERS SIMULATED WITH CMOS INVERTER

Adiabatic Logic	No. of Transistors required	Power Dissipation (Watts)			Prop. Delay (secs) at 1V	Power savings at 1V
		1V	2V	3V		
CMOS	2	51.84n	44.43u	147.8u	11.8p	-
ECRL	4	18.36n	0.501u	6.745u	8.41n	64.5%
2N2N2P	6	38.37n	0.993u	13.04u	8.42n	26%
PFAL	6	30.90n	0.990u	13.18u	8.40n	40.4%
DC-DB PFAL	7	12.40n	0.137u	1.289u	7.73n	76%
DFAL	3	15.21n	22.56u	62.94u	5.22n	70.6%
DCPAL	5	5.778n	0.027u	0.205u	8.41n	88.8%
M-QSERL	4	17.27n	7.011u	296.3u	5.29n	65.8%

TABLE III COMPARISON OF DELAY AND POWER SAVINGS OF DIFFERENT ADIABATIC INVERTERS SIMULATED WITH CMOS INVERTER

Adiabatic Logic	Prop. Delay (secs) at 1V	Power savings at 1V
CMOS	11.8p	-
ECRL	8.41n	64.5%
2N2N2P	8.42n	26%
PFAL	8.40n	40.4%
DC-DB PFAL	7.73n	76%
DFAL	5.22n	70.6%
DCPAL	8.41n	88.8%
M-QSERL	5.29n	65.8%

potential incompetence or design considerations.

Generally, as the supply voltage increases, power dissipation tends to increase across all logic families. This is expected due to the quadratic relationship between power and voltage in CMOS circuits [69]. However, the rate of increase in power dissipation varies among different logic families. Some families may exhibit steeper increases in power with voltage, highlighting differences in design and efficiency [70].

Designers can optimize their circuit by selecting logic families that offer lower power dissipation for the desired operating voltage[71]. For instance, DCPAL shows consistently low power dissipation across different voltages. Understanding the power characteristics of each logic family can help in choosing the most suitable one for a specific application, considering both performance and energy efficiency requirements[72].

Alongside power dissipation, delay is another crucial parameter in evaluating the performance of logic families. Table III demonstrates the comparison of propagation delay of different adiabatic inverters simulated with CMOS inverter. CMOS logic has the lowest delay of 11.8psec whereas DFAL and MQSERL shows relatively lower delay, indicating competitive performance in terms of speed. There often exists a trade-off between power dissipation and delay in logic design. Families with lower delay may consume more power, while those with higher delay may be more power-efficient. Integrating delay analysis with power analysis provides a holistic view of circuit performance, allowing designers to make informed decisions considering both speed and energy efficiency[73].

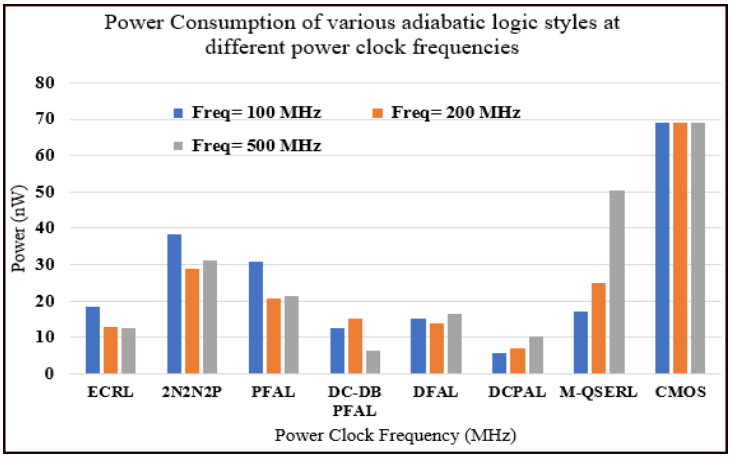


Fig. 10 Bar chart representing power consumption of adiabatic inverters at different power clock frequencies

Fig. 10 represents a comparison of power consumption of adiabatic inverters obtained at different power clock frequencies of 100 MHz, 200 MHz, and 500 MHz. It can be notably observed that as clock frequency increases keeping other variables constant, power consumption varies among adiabatic logic designs. Some may consume more power at higher frequencies, while others remain stable or even reduce power consumption[74].

DCPAL consistently demonstrates the lowest power consumption with maximum power savings of 88.8% across all clock frequencies compared to other designs. It maintains low power consumption even as the clock frequency increases, making it an efficient choice for high-speed applications, while the 2N2N2P inverter has the highest power consumption (38.37n) at 100 MHz. The power consumption of the DC-DB PFAL inverter decreases significantly from 200 MHz to 500 MHz (from 15.29n to 6.314n), indicating a potential efficiency improvement at higher frequencies.

6. FUTURE WORK

The comparative analysis of Partial Adiabatic Logic (PAL) techniques and CMOS has provided valuable insights into the strengths and limitations of these logic families in terms of power dissipation, speed, and area efficiency. While the simulation results highlight the potential of PAL techniques to reduce power consumption and offer improvements in energy recovery, they also reveal certain challenges, such as slower switching speeds and increased design complexity, which must be addressed for practical implementation.

Despite the promising results, there are still several aspects of adiabatic logic that require further exploration and optimization [76]. For example, improving the energy recovery efficiency, scalability to advanced process nodes, and clocking techniques are critical to making these techniques viable for large-scale, high-speed applications. Moreover, these circuits often require more complex designs and specialized power management techniques, potentially increasing overall circuit complexity. Additionally, the trade-offs between power, delay, and area in the context of real-world designs need to be further investigated to fully realize the potential of PAL circuits in next-generation VLSI systems.

The growing demand for low-power applications—such as IoT, industrial and medical sensors, wearable and battery-powered devices, smart lighting, and smart agriculture— continues to fuel innovation in circuit design, leading to more efficient and sustainable electronic devices. These applications require low-power microcontrollers, new energy- efficient techniques, and sleep modes to minimize energy usage while maintaining essential functionality[75].

Building on the findings from this study, future work will focus on addressing these challenges by developing more efficient PAL circuit topologies, exploring novel energy recovery techniques, and improving clocking strategies to enhance the speed and power efficiency of adiabatic logic circuits. Investigating Full energy recovery techniques and improved circuit structures that can recover a higher percentage of energy during transitions to further reduce power dissipation. Adapting PAL techniques for future nanometer process technologies, ensuring that these circuits remain effective as the industry progresses toward smaller nodes. Exploring the potential of hybrid circuits that combine CMOS or other low leakage power FinFETs with adiabatic logic to capitalize on the strengths of both technologies while mitigating their respective weaknesses. Incorporating adiabatic logic families into circuit design can thus lead to substantial reductions in power consumption, addressing the energy-conscious demands of modern electronic devices. Scalable circuit layouts with minimal power usage can be achieved through multiple-phase power clocks with integrated memory or retractile cascading power clocks[77], [78]. Additionally, new adiabatic devices using FinFETs integrated with other low power technology like GDI (Gate Diffusion Input) with

rapid switching speeds can be designed to enhance switching rates compared to CMOS logic for applications in mobile devices, IoT, and high-performance computing with reduced leakage power and overall better performance in terms of area and power consumption.

By addressing these areas, we aim to improve the practical feasibility of adiabatic logic in real-world systems, ultimately enabling their adoption in low-power, high-performance applications [79], [80].

7. CONCLUSION

The exploration of future work highlights several promising avenues for improving the practical applications of Partial Adiabatic Logic (PAL) techniques, including advancements in energy recovery, optimization for nanometer technology nodes, and the development of hybrid circuits. While these areas hold great potential, the current study has already demonstrated the foundational benefits and challenges of adiabatic logic compared to traditional CMOS.

As we look to the future, it is clear that continued research in these areas is essential to fully realize the potential of PAL techniques in low-power, high-performance applications. However, based on the insights gathered from this study, it is evident that adiabatic logic offers significant promise in addressing the power dissipation challenges of modern VLSI systems.

In this study, we have explored the performance and potential of Partial Adiabatic Logic (PAL) techniques as a means to achieve energy-efficient, low-power digital circuits. Through a detailed simulation analysis and comparative performance metrics against traditional CMOS, we have demonstrated that PAL circuits can offer significant reductions in dynamic power dissipation and improved energy recovery, though challenges such as switching speed and design complexity remain. The simulation results reveals that the adiabatic logic DCPAL and DC-DB PFAL offers significant power reduction and better performance and offer notable power savings up to 88.8% and 76% respectively, in comparison to traditional CMOS logic.

Results upto 500 MHz has been shown and adiabatic logic may well be applied in lower power computation within this frequency. However, new adiabatic design at high frequency may be targeted so that adiabatic circuit may be used in many high frequency applications also. This review will help us utilize the particular PAL technique relative to CMOS logic effectively depending on specific application requirements and trade-offs.

While further research is necessary to optimize these circuits for real-world, large-scale VLSI applications, the results of this study provide a strong foundation for the future development of adiabatic logic in high-performance, low-power systems. As the quest for ultra-low power circuit designs goes on increasing, these low-power circuit technologies would prove to be very useful in serving the need for ultra-low power circuit designing. Moving forward, the exploration of advanced energy recovery techniques, scalability for smaller technology nodes, and hybrid CMOS-adiabatic designs will be essential to realize the full potential of these circuits in next-generation technologies.

Declarations

Author contributions- Conceptualization, methodology, Investigation, analysis, preparation of the draft, review and editing, Visualization and validation

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