Pioneering Innovations in Nanoelectronics Paving the Way for Next Generation Artificial Intelligence

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This review paper presents a comprehensive analysis of the evolving integration between Nnoelectronics and Artificial Intelligence (AI), highlighting the transformative potential of nanoelectronics innovations in advancing AI capabilities. With the exponential growth of AI applications, particularly in machine learning, deep learning, and optimization, the limitations of classical computing architectures have become increasingly apparent. Nanoelectronics, including quantum computing, neuromorphic systems, and advanced memory technologies, offer novel solutions to address these challenges by enhancing computational speed, energy efficiency, and scalability. This paper explores key developments and applications of nanoelectronic devices such as memristors, quantum bits, and spiking neural networks to revolutionize AI by making it more adaptive, efficient, and robust. Although promising advances have been made, significant challenges persist, and as such this paper also discusses issues related to scalability, error correction, qubit coherence, and the integration of quantum and classical architectures. Finally, this review emphasizes the transformative impact that the fusion of these fields could have on the future of computation, leading to the development of intelligent systems capable of solving complex real-world problems faster, more efficiently, and more effectively.

Keywords: Nanoelectronics, Artificial Intelligence (AI), Quantum Computing, Neuromorphic Systems, Memristors

Graphical Abstract:
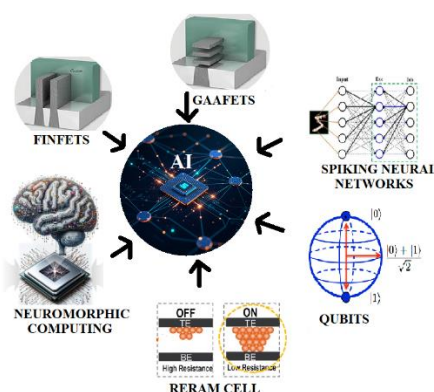
1. Introduction

The convergence of nanotechnology and artificial intelligence (AI) is opening a transformative new chapter in technology, one that promises to drive the next wave of intelligent systems [1]. Nanoelectronics, characterized by the manipulation of electronic components at the nanometer scale, has long been instrumental in the miniaturization and enhancement of electronic devices. Today, however, its implications reach far beyond conventional applications, directly influencing the capabilities, efficiency, and scalability of AI systems. As AI increasingly demands high computational power, low energy consumption, and high-speed data processing, nanoelectronics has emerged as a foundational technology capable of meeting these requirements and, consequently, redefining the landscape of machine intelligence.

AI, widely seen as a cornerstone of computer science and machine learning, traces its roots back to the mid-20th century [2]. Initial efforts in AI concentrated on symbolic logic and expert systems, aiming to imitate human thought processes. However, the field encountered multiple setbacks, caused by insufficient computational resources and overly ambitious goals. In recent years, AI has experienced a revival driven by three crucial elements: the explosion of big data, advancements in computing capabilities, and breakthroughs in algorithm design [3][4]

The digital era resulted in the generation of vast amounts of data, providing AI algorithms with an abundance of training resources. This fueled the advancement of machine learning methods, especially deep learning, which brought significant breakthroughs in fields such as image recognition, natural language processing, and reinforcement learning [5]. Improvements in hardware, such as Graphics Processing Units (GPUs) and dedicated AI chips, greatly speed up the training and deployment of AI models, turning once challenging tasks into achievable goals. At present, AI has become an integral part of our everyday life, powering everything from virtual assistants to self-driving cars and predictive healthcare technologies. Its evolution is ongoing, pushing the boundaries of what it can do in new and exciting directions.

Nanotechnology is a multidisciplinary field that originated from the discovery that materials display distinct properties at the nanoscale, typically characterized by structures smaller than 100 nanometers. Richard Feynman's iconic 1959 lecture, "There's Plenty of Room at the Bottom," provided the conceptual basis for nanotechnology, envisioning the ability to manipulate atoms and molecules at an individual level [6]. Since then, Nanotechnology has advanced significantly allowing nanomaterials and nanodevices with remarkable properties to be designed and fabricated for use in diverse fields [7].

In this review, we explore the landscape of nanoelectronics innovations that are shaping AI. We discuss key advances, address existing challenges, and outline the potential future directions where this synergy could lead. This paper highlights the transformative potential of nanoelectronics on AI and the critical role it will play in ushering in next-generation intelligence.

2. Background

Nanoelectronics, with its ability to manipulate materials at the atomic scale, offers unmatched efficiency, speed, and scalability. These advancements are not only enhancing AI performance but also enabling groundbreaking applications in areas such as autonomous systems, smart devices, and quantum computing. This synergy marks a pivotal step toward redefining the future of intelligent technologies.

2.1. Overview of Nanoelectronics

Nanoelectronics explores the fascinating interplay of electronic, atomic, and molecular dynamics at the nanoscale, centering on the creation of nanoscale films, wires, and complex assemblies. This field harnesses quantum effects to unveil the electronic traits, behaviors, and assembly processes unique to this tiny yet powerful domain. Over the past two decades, significant breakthroughs have transformed nanoelectronics, enabling ultra-small, highly efficient, and powerful devices that are revolutionizing fields from computing to biomedical technology [8]. Landmark research includes the development of silicon-based nanoscale transistors, which have been foundational in sustaining Moore's Law and pushing the limits of traditional semiconductor technology [9]. Carbon-based nanomaterials, notably carbon nanotubes (CNTs) and graphene, have further expanded nanoelectronic applications by providing materials with superior conductivity, flexibility, and mechanical strength [10]. The integration of CNTs in field-effect transistors (CNT-FETs) has shown great potential for reducing power consumption and enhancing performance, paving the way for next-generation low-power electronics [11], [12]. Additionally, the advent of quantum dots and other quantum materials has enabled new paradigms in information processing and storage, fostering the development of quantum computing and neuromorphic systems [13]. These advances are complemented by breakthroughs in nano-fabrication techniques, such as extreme ultraviolet (EUV) lithography, which have made it possible to produce increasingly intricate patterns on semiconductor materials with high precision [14]. Altogether, nanoelectronics has evolved into a multi-disciplinary field, drawing from physics, chemistry, and materials science, and promises to drive innovations in electronics for decades to come [15].

2.2. AI and Computational Demands

The development of artificial intelligence (AI) over the last two decades has led to remarkable advances in machine learning, natural language processing, and computer vision, driven by an unprecedented increase in computational capabilities. Groundbreaking innovations, such as deep learning networks, have enabled AI to achieve human-like performance in image recognition and language understanding [16], [17]. The advent of generative adversarial networks (GANs) has also transformed content generation and synthesis, introducing novel possibilities in media and creative industries [18], [19]. However, as AI models have grown in complexity—from early neural networks to today's large-scale transformers like GPT-3, which utilizes 175 billion parameters [20]—the computational demands have surged exponentially. Meeting these demands has necessitated cutting-edge advancements in hardware, such as graphics processing units (GPUs) and tensor processing units (TPUs), designed specifically to accelerate deep learning workloads [21]. Furthermore, researchers are exploring alternative computing paradigms, including quantum computing, as a potential solution to the escalating resource requirements of AI models [22]. The convergence of AI and high-performance computing is driving not only the continued expansion of AI capabilities but also renewed investigations into energy-efficient architectures to mitigate the environmental impacts of large-scale model training [23]. Collectively, these advancements underscore a rapidly evolving field where computational innovation is central to sustaining AI's growth and addressing its future challenges.

Researchers are actively exploring ways to integrate nanoelectronic components seamlessly into larger AI frameworks, enhancing system efficiency and enabling advanced functionalities. As new breakthroughs emerge, the relationship between nanoelectronics and AI is expected to deepen, forging a synergistic pathway toward systems that are not only faster and more efficient but also capable of mimicking human cognitive abilities with unprecedented fidelity. Nanoelectronic components, such as nanoscale transistors and

quantum dots, offer unparalleled precision and scalability, complementing AI algorithms to enhance computational power. This convergence drives innovations in areas like neuromorphic computing, advanced robotics, and biomedical diagnostics, paving the way for intelligent systems that mimic human cognition while operating on minimal energy and space requirements. The further discussion explores major research advancements across various nanoelectronic components, examining their roles in driving innovations and enhancing the capabilities of artificial intelligence, one aspect at a time. Figure 1 showcases the key nanoelectronic devices driving the evolution of artificial intelligence.
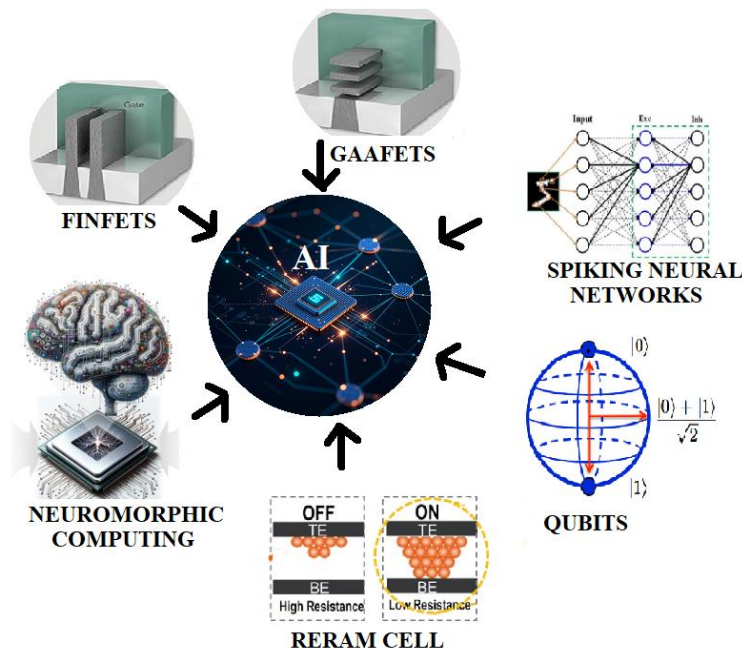

Figure 1: Advanced Nanoelectronic Devices Enabling the Development of Next-Generation Artificial Intelligence Systems

3. Advancements in Transistor Technology

Transistor technology has undergone a series of transformative advancements in recent years to meet the computational demands of artificial intelligence (AI), driving both performance and efficiency in AI hardware. The traditional silicon-based transistor, the fundamental building block of microelectronics, has been engineered to achieve increasingly smaller geometries, with the advent of FinFETs marking a pivotal step toward denser, faster, and more power-efficient devices [24], [25]. As FinFET technology reaches its scaling limits, the semiconductor industry has embraced gate-all-around (GAA) transistors, which offer improved electrostatic control, reducing leakage currents and enhancing energy efficiency in high-performance computing tasks essential for AI [26]. Figure 2 illustrates the comprehensive evolution of MOSFET technology, showcasing the development history and the latest emerging trends across various transistor architectures and scaling stages. It provides a detailed overview of how MOSFET designs have progressed over time and adapted to meet the demands of modern scaling challenges and advanced applications.
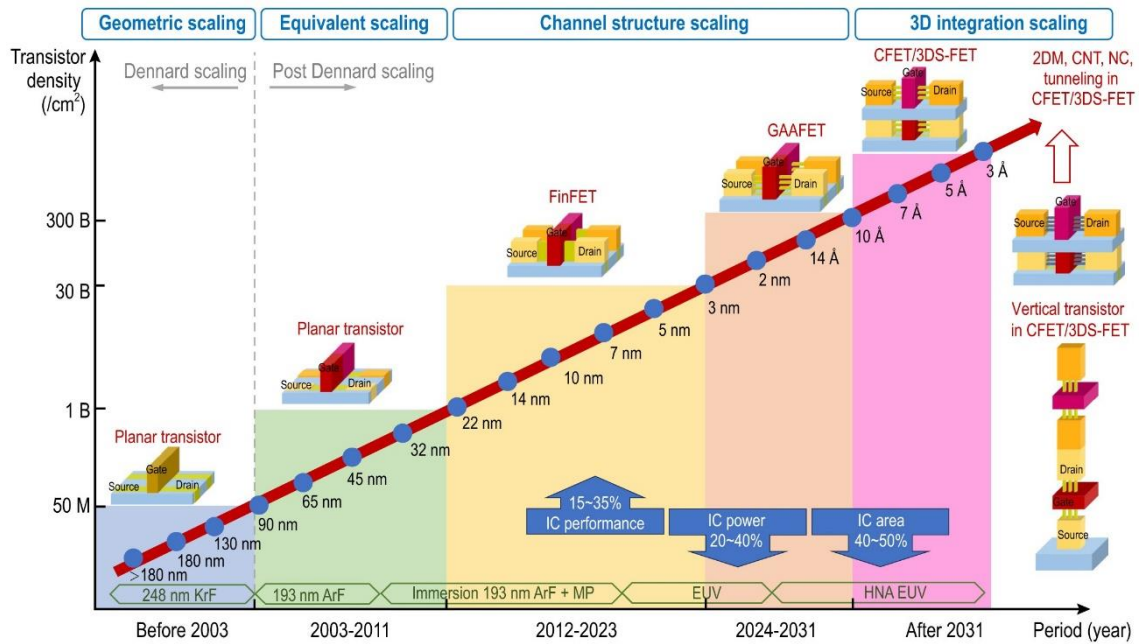
Figure 2 Evolution and emerging trends of MOSFETs across various transistor architectures and scaling stages [27]

In addition to these structural innovations, new materials are being explored to augment transistor capabilities; silicon carbide (SiC) and gallium nitride (GaN) transistors, for instance, have shown promise in reducing power consumption and improving thermal performance, critical for data-intensive AI applications [28]. Moreover, beyond traditional materials, researchers are increasingly focusing on two-dimensional (2D) materials like molybdenum disulfide (MoS_2) and graphene, which have excellent electron mobility and can support ultra-thin, flexible transistors with minimal power leakage, potentially enhancing future AI hardware [29][30] . Complementary to these developments, neuromorphic computing has emerged as a novel approach, utilizing memristive devices and other non-volatile memory technologies that mimic the neural architectures of the human brain, thereby enabling highly efficient pattern recognition and learning tasks in AI [31]. Such neuromorphic transistors not only promise drastic reductions in energy consumption but also provide a scalable path toward implementing AI models that require real-time, edge-based inference [32]. Altogether, these advancements in transistor technology underscore an interdisciplinary effort to create purpose-built hardware that can sustain the ever-growing computational and efficiency needs of AI, highlighting a field poised for continued innovation. Table 1 provides an overview of the key research developments in transistors designed for artificial intelligence applications.

Table1: Research Advances in Transistor Technologies for Artificial Intelligence Applications

Nano-transistors	Research Work	Reference
Nanowire Field-Effect Transistors (NW FETs)	NWFETs based hardware-implementable neural network (HNN) developed for tactile data processing in electronic skin (e-skin)	William Taube Navaraj et. al. [33]
Graphene-Based Field-Effect Transistors	Silver gel/polarized-aptamer is introduced as gate	Chuan Yu Han et. al. [34]

	dielectric to mimic synapse function.	
2D MoS$_2$ field effect transistor	An optoelectronic memory from a 2D layered MoS2 transistor show that the combination of gate voltage and light can enable a multilevel memory device.	Arum Kumar et. al. [35]
Tunneling Field-Effect Transistors (TFETs)	TFETs hybridized with the memristor for better execution of combinational and sequential circuits	Jeetendra Singh et. al. [36]
Quantum Dot Photosynaptic Transistors	Perovskite quantum dots engineered for advancing neurologically soft optoelectronics and neuromorphic computation.	Wei Cheng Chen et. al.[37]
Spintronic Transistors	Improves non-volatile AI memory applications, critical for AI-enabled IoT systems.	Jorge Puebla et. al. [38]

3.1. Fin Field-Effect Transistors

Fin Field-Effect Transistors (FinFETs) technology represents a groundbreaking evolution in transistor architecture, addressing the limitations of traditional planar transistors as scaling reaches the nanometer regime. Introduced commercially in the early 2010s, FinFETs feature a three-dimensional (3D) structure, where the silicon channel is raised into a "fin" shape, allowing the gate to wrap around three sides of the fin as shown in Figure 3 [39], [40]. This geometry improves electrostatic control over the channel, effectively reducing leakage currents and enhancing switching speeds—key challenges in planar transistor designs at smaller nodes [41]. FinFETs became a critical component in enabling Moore's Law to continue beyond the 20-nanometer node, as the 3D structure mitigates short-channel effects, which degrade transistor performance and power efficiency at ever-shrinking scales. Consequently, FinFET technology has fueled the production of faster and more energy-efficient integrated circuits (ICs), particularly in high-performance computing and mobile devices where efficiency and speed are essential [42].
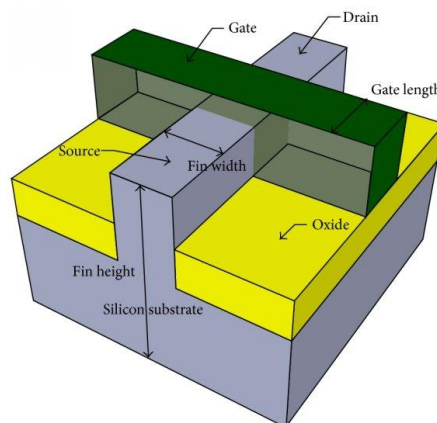

Figure 3: Basic structure of FinFET [43]

In addition to performance improvements, FinFETs offer significant benefits for scaling in both logic and memory applications. With their ability to maintain excellent control over channel formation, FinFETs can sustain operational integrity and reduce power consumption across a wide voltage range, a critical factor for battery-dependent applications [26]. Research has shown that FinFET devices can reduce static power consumption by nearly half compared to planar counterparts, a breakthrough for systems-on-chip (SoC) and other applications demanding low-power consumption [44]. These advancements have been pivotal in meeting the rising demand for energy-efficient AI hardware, as FinFET technology provides the foundation for high-density transistor layouts that support complex AI and machine learning models.

FinFETs are expected to be replaced by GAA NW-FETs as technology scales down to 5 nm, but shrinking further to 3 nm brings new challenges. To handle these, nanosheet FETs (NS-FETs) are emerging as a better option. NS-FETs are designed to work efficiently at very small sizes (below 5 nm) by reducing performance issues like short channel effects (SCEs). This makes them important for continuing the progress of advanced circuits and keeping Moore's Law alive [45]. Figure 4 illustrates the 3D configurations of (a) FinFET, (b) stacked NW-FET, and (c) vertically stacked NS-FET, showcasing their distinct structural characteristics. The FinFET architecture is characterized by a fin-like structure with the gate enveloping the fin to achieve superior electrostatic control. In contrast, the stacked NW-FET employs multiple layers of cylindrical nanowires, each encased by a surrounding gate, optimizing current flow and device performance. The vertically stacked NS-FET features horizontally oriented nanosheets arranged in a stacked configuration, with gates encircling each sheet, offering significant advancements in scaling and overall device efficiency. These designs enable further miniaturization while maintaining the excellent control over current seen in FinFETs. Such advancements are crucial for advancing semiconductor technology to meet the growing demand for AI applications that require powerful yet energy-efficient performance. The shift from FinFETs to newer architectures like gate-all-around FETs represents a continuous evolution, ensuring semiconductor devices remain capable and innovative for the future, highlighting the lasting importance of FinFET technology in modern electronics [27].
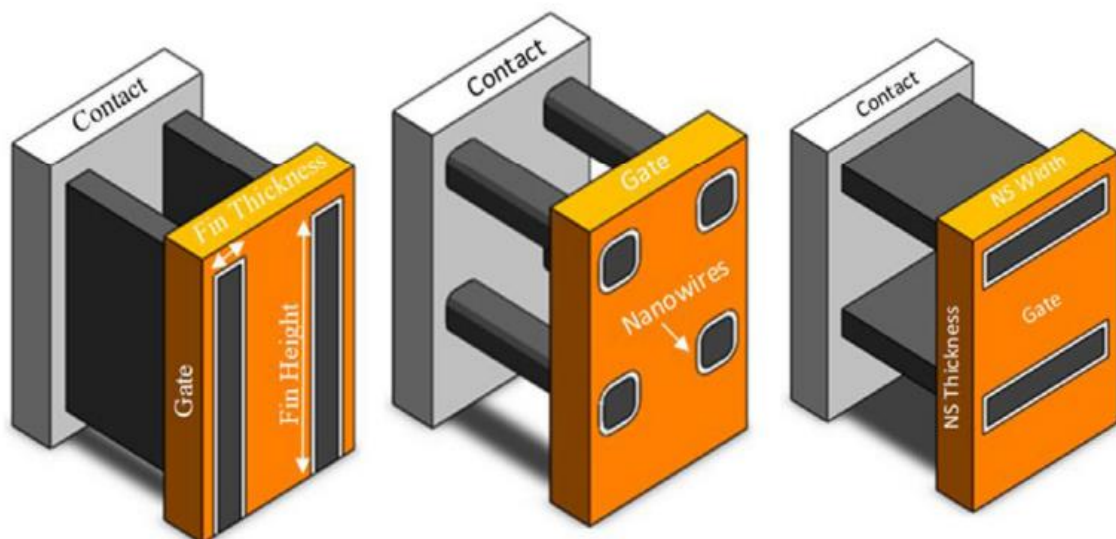

Figure 4: 3D representations of (a) FinFET, (b) stacked NW-FET, and (c) vertically stacked NS-FET [45]

3.2. Gate-All-Around Transistors

Gate-All-Around (GAA) transistors technology marks a significant milestone in the continued miniaturization and performance enhancement of semiconductor devices, following the scaling limitations of FinFETs [46]. GAA transistors, introduced as an evolutionary response to the need for more precise channel control at nanoscales, feature a gate that surrounds the channel entirely on all sides. This design maximizes electrostatic control over the channel, effectively reducing leakage currents and short-channel effects that limit FinFETs performance at sub-5-nanometer nodes [47]. The GAA architecture allows for the creation of nanosheet or nanowire-based structures that provide improved scalability while maintaining high current drive, a fundamental requirement for powering dense, high-performance computing applications in artificial intelligence and beyond [48].

GAA technology has demonstrated the potential to further extend Moore's Law by enabling tighter transistor packing and enhanced power efficiency. With GAA nanosheet transistors, semiconductor manufacturers can fine-tune the width of the nanosheets to optimize the performance and power characteristics of each transistor—a flexibility that was limited in FinFET designs [49]. For example, Samsung and Taiwan Semiconductor Manufacturing Company have developed GAA transistors for their 3nm process nodes, achieving remarkable reductions in power consumption and gains in speed compared to prior FinFETs-based nodes [50], [51], [52]. Such advancements have been pivotal for AI and machine learning applications, which require intensive processing power with lower thermal budgets. The energy-efficient characteristics of GAA transistors make them highly suitable for integration into modern, data-driven systems where efficiency is paramount.

Moreover, the GAA architecture is paving the way for innovations in transistor design beyond conventional materials and scaling. Researchers are exploring stacked nanosheet and nanowire transistors based on GAA principles having the designs that uses vertical stacking to increase density while managing power use and heat generation effectively [53], [54]. Figure 5 illustrates the structure and cross-sectional view of GAA-FET and Multi-Channel FET, featuring Si-Nanowire and Si-Nanosheet channels. This approach is essential as semiconductor manufacturing approaches the physical limits of 2D scaling. The GAA model's modularity allows for adaptability with emerging materials, such as 2D transition-metal dichalcogenides, which offer ultra-thin channels that could further reduce leakage currents and boost on-off current ratios[55]. In this way, GAA transistors represent a crucial step in the evolution of transistor technology, supporting the continued growth of computationally demanding fields like artificial intelligence while adhering to stringent power efficiency requirements.
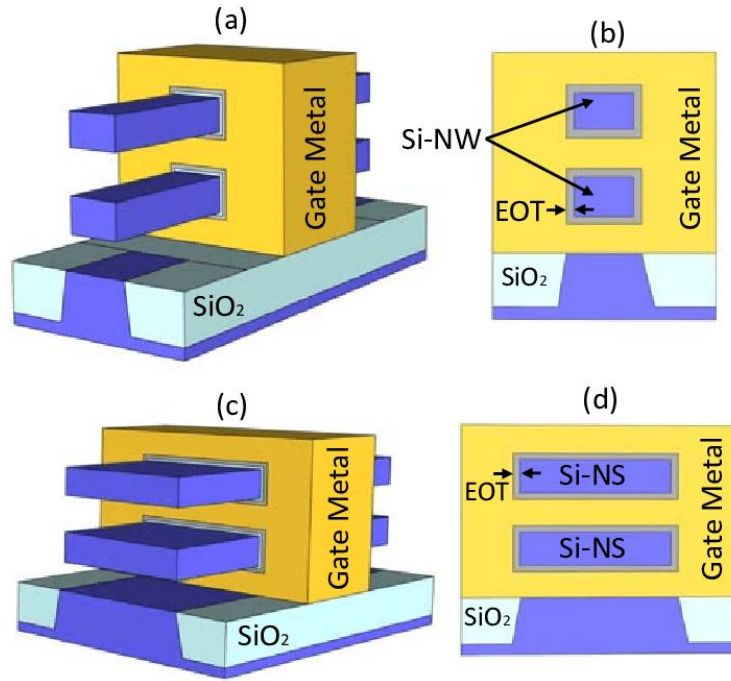
Figure 5: GAA-FET: (a) Structure and (b) cross-sectional view with Si-Nanowire (NW) channel. MBC-FET: (c) Structure and (d) cross-sectional view with Si-Nanosheet (NS) channel [54]

4. Memory Devices and Storage

Memory devices and storage technologies play an essential role in the advancement of artificial intelligence (AI), providing the rapid access and large capacity needed to handle increasingly complex datasets and sophisticated models. As AI algorithms, particularly in deep learning, require high data throughput and low-latency memory to perform efficiently, innovations in both volatile and non-volatile memory have been critical to AI development. Traditional DRAM, while fast, faces scalability and power limitations in meeting the needs of AI workloads, spurring interest in alternative memory technologies such as resistive random-access memory (ReRAM), phase-change memory (PCM), and magnetoresistive random-access memory (MRAM) [56], [57]. These emerging non-volatile memories combine speed with data retention capabilities, offering improved energy efficiency and durability, which are essential for intensive AI applications [58]. Additionally, advancements in storage technology, including solid-state drives (SSDs) and storage-class memory (SCM), have revolutionized data handling, enabling faster data access and efficient caching mechanisms that directly impact AI training and inference speeds [59]. The continued evolution of memory and storage technologies is thus integral to meeting the performance demands of modern AI systems, driving innovations in both hardware and architecture design that enhance overall system efficiency and capability.

4.1. Non-Volatile Memory Technologies

Non-volatile memory (NVM) technologies have become increasingly critical to modern computing, especially with the growing demands of data-intensive applications like artificial intelligence (AI), which require both high-speed access and persistent data retention. Traditional memory technologies, such as dynamic random-access memory (DRAM), struggle to balance speed, energy efficiency, and scalability for AI applications. Consequently, alternative NVMs, including resistive random-access memory (ReRAM), phase-change memory (PCM), and magnetoresistive random-access memory (MRAM), have emerged as viable solutions. ReRAM, for instance, utilizes metal oxides to store data through

resistance changes, offering high-speed data access and reduced energy consumption compared to conventional storage [60]. Similarly, PCM leverages the reversible phase changes in chalcogenide materials to encode data, providing fast read/write speeds with greater endurance and scalability, suitable for caching and neural network storage applications [61].

Among the most promising NVM technologies, MRAM has gained attention due to its potential to deliver high speed, endurance, and non-volatility. MRAM stores information through magnetic states rather than electrical charge, making it particularly robust for repeated read/write cycles without data degradation [62]. This robustness has led to innovations in spin-transfer torque (STT-MRAM), which further enhances MRAM's performance by allowing more efficient magnetic switching, making it a compelling candidate for AI hardware where energy efficiency and durability are paramount [63]. The high endurance of STT-MRAM is especially valuable for edge-based AI applications, which require local, non-volatile storage that can endure frequent updates without sacrificing data integrity or power efficiency.

In addition to these advances, the integration of NVM technologies into computing architectures marks a paradigm shift toward in-memory computing, where processing occurs within the memory itself rather than in a separate processing unit. This architectural approach, explored with ReRAM and PCM, promises to drastically reduce latency and power consumption by minimizing data movement between memory and processors [64]. This innovation is particularly beneficial for AI and machine learning workloads, which involve repetitive matrix operations that can be performed directly in memory. The development of in-memory computing architectures, supported by non-volatile memory, thus represents a transformative step in computing, enabling future AI systems to operate with greater efficiency, speed, and scalability. Together, these advancements in NVM technologies not only meet the increasing storage and processing demands of AI but also set the foundation for sustainable, high-performance computing in an era of exponential data growth.

4.2. Memristors

Memristors, a novel class of non-volatile memory devices, have gained substantial interest in the field of neuromorphic computing due to their unique ability to emulate synaptic functions. Unlike traditional transistors, memristors can retain information even when power is removed, and their resistance can be tuned to represent different weight values in neural networks. This makes them well-suited for analog computations essential to neuromorphic architectures, where memory and processing are co-located, mimicking the structure of the human brain. Since the initial demonstration of memristor behavior by HP Labs in titanium dioxide-based devices, significant research has focused on enhancing their scalability, switching speed, and durability [65]. Advances in materials science, such as the use of hafnium oxide and other transition metal oxides, have improved memristor performance, supporting high-density memory applications and allowing for the efficient storage of analog weights in large-scale neural networks [66].

In the context of neuromorphic computing, memristors enable the development of energy-efficient architectures that can handle massive amounts of data without the bottlenecks associated with traditional von Neumann systems, where data transfer between separate memory and processing units creates latency and power inefficiencies. Memristor-based neuromorphic chips can perform parallel computations at low power, making them highly suitable for real-time, edge-based AI applications, such as sensory processing in autonomous vehicles and IoT devices [32]. Furthermore, memristor arrays have been employed to implement hardware-based artificial neural networks, where each memristor acts as a

synapse, adjusting its conductance to represent the strength of synaptic connections. This approach significantly reduces the energy and time required for machine learning tasks, opening avenues for high-speed and low-power inference in AI systems [67].

As memristors continue to mature, researchers are exploring their potential in spiking neural networks (SNNs), a form of neuromorphic computing that leverages timing-based information similar to biological neurons. In SNNs, memristors can facilitate temporal information processing and adapt their resistance in response to incoming electrical pulses, enabling more dynamic and biologically plausible computations [68]. Additionally, hybrid architectures combining memristors with other nanoscale devices, such as resistive random-access memory (ReRAM), are being investigated to create more versatile and powerful neuromorphic systems capable of complex pattern recognition and sensory processing [69]. The convergence of memristor technology with neuromorphic computing represents a transformative shift in AI hardware, providing a foundation for the next generation of computing systems that are not only more efficient but also closer in function to the human brain, driving innovations across AI applications from robotics to healthcare.

5. Neuromorphic Computing

Neuromorphic computing is an emerging field in artificial intelligence (AI) that aims to replicate the brain's structural and functional principles to achieve unprecedented efficiency in processing power and energy consumption. Unlike traditional von Neumann architectures, which separate memory and processing units, neuromorphic computing integrates these elements in a design inspired by neural networks, thereby reducing data movement bottlenecks and enabling massively parallel processing. Pioneering research in this field has demonstrated that neuromorphic hardware can perform complex tasks such as image recognition, sensory processing, and pattern recognition with orders of magnitude less energy than conventional processors [70] [71]. This energy efficiency is achieved through the use of spiking neural networks (SNNs), which emulate the spiking activity of biological neurons, enabling event-driven processing that closely mirrors natural information flow [72]. By harnessing the unique characteristics of memristors, resistive random-access memory (ReRAM), and other non-volatile memory technologies, neuromorphic computing is not only transforming edge AI applications but also holds promise for advancing real-time processing in robotics, autonomous vehicles, and IoT systems where power and latency constraints are critical.

5.1. Brain-Inspired Architectures

Brain-inspired architectures, or neuromorphic computing systems, seek to replicate the functional dynamics and structural principles of the human brain to achieve unprecedented computational efficiency and adaptability. These architectures differ fundamentally from traditional computing models by integrating memory and processing units, allowing for parallel, event-driven processing that more closely resembles neural activity. This approach offers significant advantages for tasks involving sensory processing and real-time decision-making, which require rapid responses and high adaptability. Leading neuromorphic hardware such as IBM's TrueNorth and Intel's Loihi chips have demonstrated the feasibility of implementing SNNs at scale, achieving high energy efficiency and robustness in pattern recognition and sensory fusion tasks with power consumption significantly lower than traditional architectures [73][71] .

In addition to efficiency, brain-inspired architectures are uniquely suited to learning and adaptation in real-time environments, which is crucial for advanced artificial intelligence applications. Leveraging hardware components such as memristors, resistive random-access

memory (ReRAM), and phase-change memory (PCM), these architectures support plasticity mechanisms that emulate synaptic learning, thereby enabling devices to adapt their processing patterns based on past inputs [74], [75], [76]. For instance, memristor-based neuromorphic systems can dynamically adjust their conductance in response to neural signals, effectively mimicking synaptic weight adjustments seen in biological neurons [77]. This capability allows neuromorphic systems to perform unsupervised learning, which is invaluable in applications requiring autonomous adaptability, such as autonomous vehicles, robotic control, and environmental monitoring. By facilitating real-time learning with minimal power requirements, brain-inspired architectures are not only broadening the capabilities of AI but are also paving the way for highly adaptive, intelligent systems that can operate efficiently in diverse and unpredictable environments.

Research into brain-inspired architectures continues to expand, exploring hybrid designs that combine traditional digital components with analog and non-volatile memory elements, enhancing computational flexibility and scalability. Hybrid neuromorphic designs, incorporating elements such as silicon-based neurons with nanoscale memory devices, enable scalable and efficient representations of complex neural networks capable of higher-order cognitive tasks [78]. These advancements highlight a paradigm shift in computing where the limitations of conventional architectures are being overcome by designs that prioritize adaptability, resilience, and energy efficiency—qualities essential for the next generation of AI. As neuromorphic computing continues to progress, its integration with other advanced technologies, such as quantum computing and machine learning, promises to further revolutionize AI, bringing us closer to achieving the goal of creating intelligent systems with human-like cognitive abilities.

5.2. Spiking Neural Networks

Spiking Neural Networks (SNNs) represent a paradigm shift in artificial neural network design, inspired by the brain's biological neural processing. Unlike traditional artificial neural networks, which rely on continuous signals to propagate information, SNNs model neurons that communicate by transmitting discrete spikes or action potentials at precise moments in time. Figure 6 represents the basic SNN architecture in which there is an input layer that encodes input pixels into spikes and connects fully to the excitatory (Exc) neuron layer and the processing layer operates on a winner-take-all principle, utilizing a specific connection pattern between excitatory neurons and inhibitory (Inh) neurons to produce a lateral inhibition effect. Spiking neural networks (SNNs), a key component of brain-inspired computing, simulate the timing-based firing patterns of biological neurons, where spikes convey information through their precise timing rather than continuous values, enabling efficient, low-power computations [79]. Leveraging spike-timing-dependent plasticity (STDP), a learning rule that adjusts synaptic strengths based on the timing of neural spikes, spiking neural networks (SNNs) exhibit adaptive learning capabilities. This allows them to effectively perform complex tasks such as recognizing patterns, processing sensory inputs, and making dynamic decisions in real time [80]. These features make SNNs particularly well-suited for applications where real-time processing and low-power operation are critical, such as robotics, autonomous systems, and edge computing.
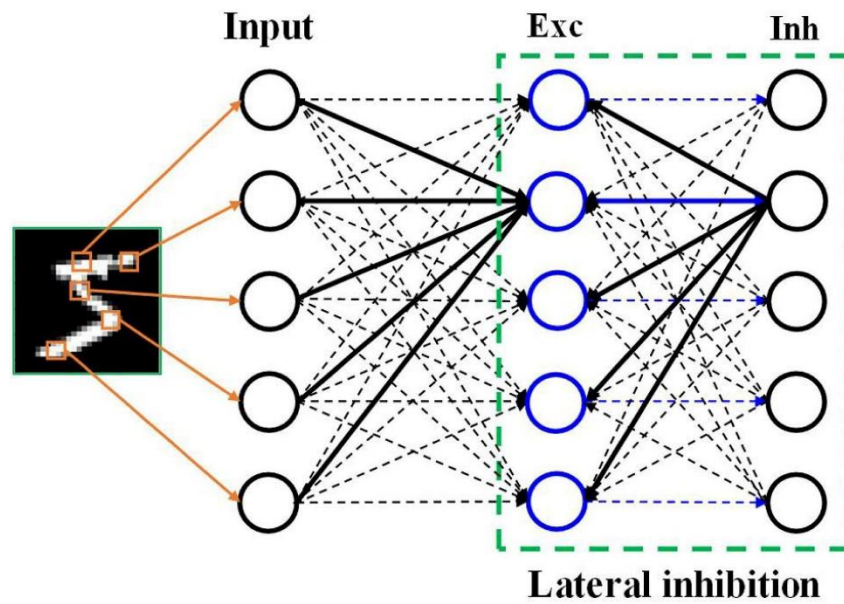
Figure 6: SNN architecture [81]

The development of hardware to support SNNs has made significant strides in recent years, with neuromorphic computing systems offering the necessary infrastructure to implement large-scale SNNs efficiently. Memristors, resistive random-access memory (ReRAM), and other emerging non-volatile memory technologies play a central role in neuromorphic hardware by enabling the storage and modification of synaptic weights in a manner that is both energy-efficient and scalable [82]. These advancements have propelled SNNs into real-world applications, including sensory processing in robotics, where the ability to process time-sensitive signals in real time is critical for decision-making and motor control. Furthermore, SNNs excel in applications that require continuous learning in dynamic environments, making them ideal for autonomous systems and AI at the edge.

Despite these advancements, the implementation of large-scale, biologically plausible SNNs still faces challenges in terms of scalability, training methods, and computational complexity. Traditional training algorithms, which rely on backpropagation in conventional artificial neural networks, are not directly applicable to SNNs due to their discrete and event-based nature [83]. As a result, researchers are developing novel learning algorithms tailored to the spiking nature of SNNs, such as spike-time-dependent plasticity (STDP) and reward-modulated learning, which enable SNNs to learn in a more biologically plausible manner [84]. Additionally, efforts to optimize hardware for SNNs are focused on improving the integration of analog and digital components to reduce power consumption and enhance the speed of spike-based computations. These challenges, however, also present exciting opportunities for innovation in both software and hardware, as the quest to develop scalable, efficient, and biologically inspired learning systems continues to drive the future of AI. The convergence of these advancements in SNNs promises to usher in a new era of highly adaptive, energy-efficient AI systems capable of performing cognitive tasks with human-like flexibility and efficiency.

Quantum Gates and Qubits
Quantum computing and artificial intelligence (AI) are two revolutionary domains that are reshaping technology and science. Quantum computing harnesses the principles of quantum mechanics to perform computations far beyond the capabilities of classical systems. When integrated with AI, it holds the potential to accelerate problem-solving, optimize complex

systems, and unlock new possibilities in areas like machine learning, natural language processing, and data analytics.

Quantum gates and qubits represent the core elements of quantum computing, a field that holds significant potential for advancing artificial intelligence (AI) through enhanced computational power. Qubits, the fundamental units of quantum information, differ fundamentally from classical bits in that they can exist in multiple states simultaneously due to the phenomenon of superposition. This ability allows quantum computers to process a vastly larger amount of information in parallel compared to classical systems. In quantum computing, quantum gates perform operations on qubits [85], manipulating their states through quantum mechanical phenomena such as superposition and entanglement [86]. Unlike classical logic gates, which perform deterministic operations on bits, quantum gates act probabilistically, enabling a higher degree of complexity and potential speed in performing computational tasks [87]. The ability of quantum gates to execute operations in parallel offers a powerful mechanism for accelerating AI algorithms through quantum processors, particularly in tasks involving large-scale data analysis, optimization, and machine learning, where traditional computing methods face limitations in processing speed and scalability. Figure 7 presents one such physical quantum processor.
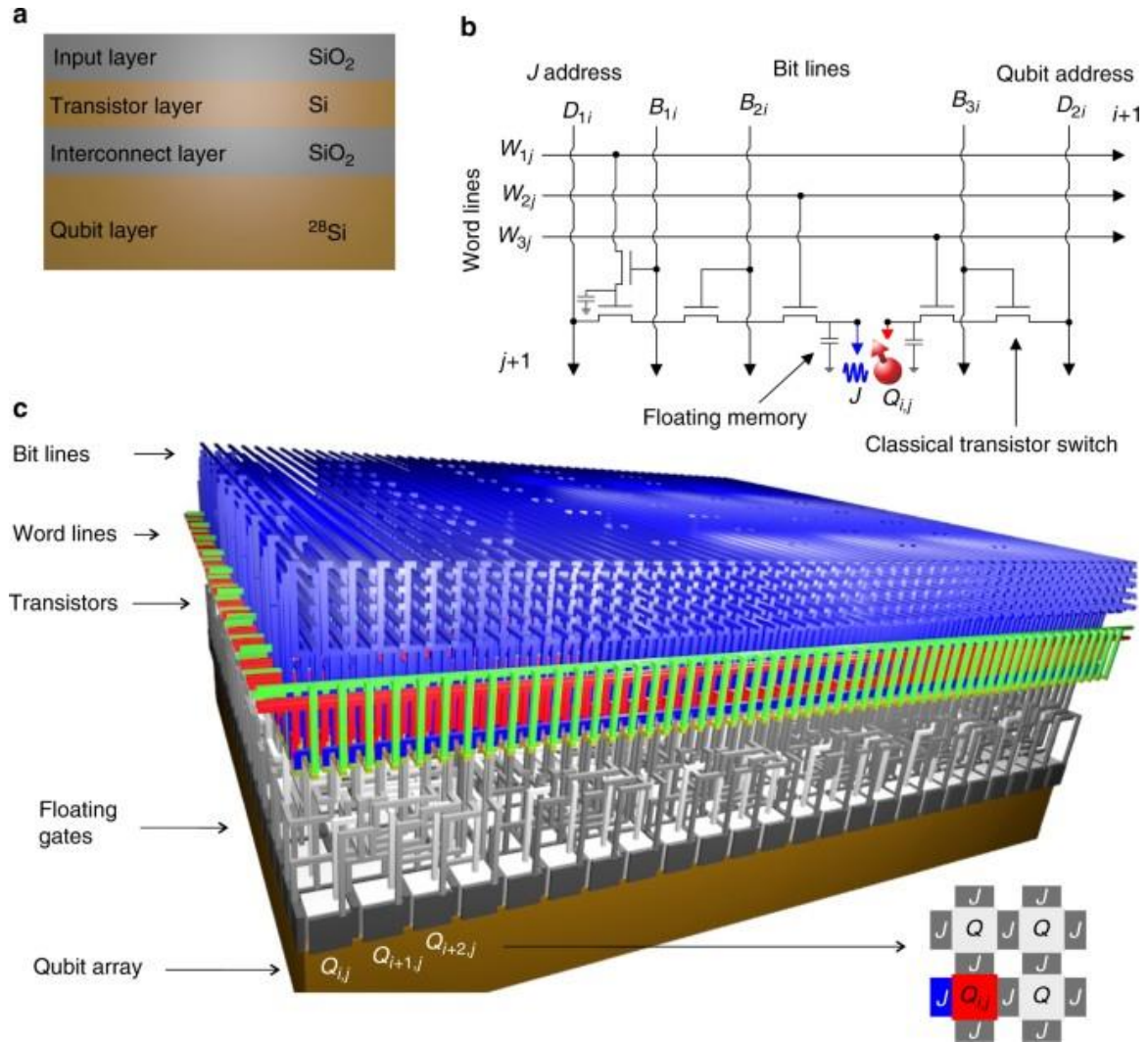

Figure 7: Physical quantum processor (a) A silicon-on-insulator (SOI) wafer where the bottom layer, made of isotopically enriched silicon-28, hosts the 2D qubit array, while the top

silicon layer contains transistors for qubit operation. These components are interconnected through oxide regions using polysilicon or other metal vias. (b) An electrical circuit designed to control one Q-gate and one J-gate, enabling individual, row-by-row, or global operations as detailed in the main text. (c) The physical architecture of a unit module comprising 480 qubits. The inset at the bottom right provides a plan view cross-section of the qubit plane, showing each J-gate and qubit connected via the circuit depicted in (b). [88]

In AI development, the promise of quantum computing lies in its potential to solve problems that are computationally intractable for classical computers. Quantum gates, through operations like the Hadamard gate, CNOT gate, and Toffoli gate, enable entanglement—the quantum phenomenon where qubits become correlated such that the state of one qubit directly affects the state of another, even at great distances [89]. This property of entanglement can be harnessed to create quantum neural networks and improve optimization algorithms that are crucial for AI tasks like training deep learning models, solving combinatorial optimization problems, and enhancing pattern recognition [90]. Quantum-enhanced algorithms, such as the Quantum support vector classification (QSVC) and Quantum support vector regression (QSVR), offer significant speedups for specific AI tasks by using simulated and real quantum processors. Results show that QSVC performs well despite noise, while low-rank approximations and hyperparameter tuning enhance QSVR accuracy on noisy devices, highlighting the robustness of quantum kernels for diverse datasets [91]. Thus Quantum computers explore vast solution spaces with greater efficiency compared to classical counterparts.

The development of quantum gates and qubits for AI is still in its nascent stages, with significant challenges remaining in terms of qubit coherence, error rates, and scalability. Quantum hardware is susceptible to noise and decoherence, which can degrade the accuracy and reliability of quantum operations, particularly when qubits are entangled for extended periods. Nonetheless, recent advancements in quantum error correction and fault-tolerant quantum computation have made strides toward mitigating these issues, with the development of surface codes and topologically protected qubits offering promising solutions [92]. Additionally, the hybridization of quantum and classical computing, known as quantum-classical algorithms, is emerging as a practical approach to leverage the strengths of both paradigms. By using quantum gates to perform certain computationally intensive tasks and classical systems for others, researchers are developing more feasible pathways for incorporating quantum computing into AI applications, pushing the boundaries of what is achievable in machine learning, cryptography, and large-scale data processing. The convergence of quantum computing and AI holds immense promise, offering a transformative leap in computational power that could redefine the future of intelligent systems.

Future scope in Convergence of Nanoelectronics and AI

The convergence of nanoelectronics and artificial intelligence (AI) depends on creating energy-efficient, high-performance systems that leverage advanced nanomaterials. However, integrating nanoelectronics with AI presents significant challenges, including material limitations and system-level complexities. A key issue is maintaining performance and reliability at the nanoscale. Additionally, integrating AI algorithms with nanoelectronic systems requires a fundamental shift in computational design, as traditional architectures built for silicon-based systems must be restructured. This involves harnessing parallelism, quantum coherence, and non-linearity while redesigning hardware-software interfaces. Addressing these challenges is crucial to bridge the gaps between material science, computational theory, and system engineering for the development of next-generation AI-driven nanoelectronic devices. Here is the discussion about some of the major the challenges

that is needed to bridge the gap between material science, computational theory, and system engineering towards the development of high performance nanoelectronics devices for advanced AI applications.

i. **Scalability and Fabrication Challenges**: The integration of nanoelectronics with artificial intelligence (AI) faces significant challenges in scaling up from laboratory prototypes to large-scale, reliable systems. Nanoelectronics, particularly at the nanoscale, suffer from issues like variability in device performance, which complicates the manufacturing process. As device dimensions approach atomic scales, quantum effects become more pronounced, making it difficult to maintain predictable behavior. Furthermore, the advanced fabrication techniques required for nanoelectronics often involve complex and costly processes, making mass production challenging [93]. The transition from research-scale devices to commercially viable AI hardware remains a significant hurdle.

ii. **Quantum Coherence and Stability in Qubits**: Quantum computing, which is poised to revolutionize AI through enhanced computational power, faces the issue of qubit coherence and stability. Qubits, the building blocks of quantum AI, are extremely sensitive to environmental noise, leading to errors in computations. Maintaining coherence over long periods, necessary for complex AI algorithms, remains an unsolved problem in quantum hardware. Current quantum error correction methods, while promising, are still in the developmental stages and add significant overhead to quantum computations [94]. These limitations hinder the full integration of nanoelectronics-based quantum systems with AI applications, particularly in tasks requiring high reliability and precision.

iii. **Energy Efficiency and Heat Dissipation**: One of the major challenges in integrating nanoelectronics with AI is managing the energy efficiency and heat dissipation of nanoscale devices. AI algorithms, particularly deep learning models, require substantial computational resources, leading to high power consumption. While nanoelectronics promise reduced energy usage due to smaller transistor sizes, they also face challenges related to heat generation as device density increases [95]. Efficient cooling mechanisms and low-power operation are crucial for maintaining the performance of AI hardware, especially as the complexity of AI models continues to grow. Balancing energy consumption with performance is a key challenge that must be addressed for scalable AI solutions [96].

iv. **Interfacing Nanoelectronics with Classical AI Systems**: The integration of nanoelectronics with classical AI systems, such as neural networks and deep learning models, presents challenges in terms of compatibility and communication [97]. Nanoelectronics-based systems, such as memristors or quantum circuits, often operate using different principles from traditional digital logic circuits. The design of hybrid systems that can seamlessly interface between quantum or neuromorphic components and conventional AI hardware is a non-trivial task. Interfacing between classical and quantum systems, for instance, introduces issues of signal translation, data conversion, and latency, which need to be addressed for efficient system operation [98]. Developing standardized communication protocols for hybrid systems remains a significant research area.

v. **Designing Algorithms for Quantum and Neuromorphic Systems**: Developing AI algorithms that can fully exploit the potential of quantum and neuromorphic systems is a

significant challenge. Traditional AI algorithms, designed for classical computers, do not map directly onto quantum or neuromorphic architectures. Quantum AI algorithms, such as Quantum Approximate Optimization Algorithm (QAOA), require fundamentally different approaches to problem-solving, making it difficult to adapt existing AI models to take advantage of quantum speedups [99]. Similarly, neuromorphic computing, inspired by the brain's structure, requires new models that can handle the asynchronous, event-driven processing of spiking neural networks [100]. Developing specialized algorithms that can leverage the unique properties of nanoelectronics-based AI hardware remains an open challenge.

vi. **Noise and Error Correction in Neuromorphic Systems**: In the realm of neuromorphic computing, integrating nanoelectronics such as memristors with artificial neural networks also faces challenges related to noise and error correction [101]. Memristor-based devices, which are central to neuromorphic systems, are prone to variations in their resistance states, especially at the nanoscale [102]. These variations can introduce errors in the learning and memory processes, which undermine the reliability of neuromorphic systems for complex AI tasks. Developing robust error-correction techniques to handle noise in memristor-based circuits, while ensuring that these systems maintain low power consumption, is essential for scaling up neuromorphic AI solutions.

vii. **Material Limitations and Device Heterogeneity**: The development of nanoelectronics for AI also faces material limitations. As researchers explore new materials for quantum and neuromorphic systems—such as topological insulators, two-dimensional materials, and superconducting qubits—there are significant challenges related to material consistency, integration, and heterogeneity. Variations in material properties can lead to inconsistent device performance, complicating the integration of different nanoelectronic components into a cohesive AI system [103]. Additionally, the need for precise control over fabrication processes to maintain the quality of materials adds another layer of complexity to scaling up nanoelectronics for AI. By addressing these challenges, researchers can unlock the full potential of nanoelectronics and AI, leading to more efficient, scalable, and powerful systems capable of solving complex, data-intensive problems in fields ranging from healthcare to autonomous systems.

6. Conclusion

In conclusion, the intersection of nanoelectronics and artificial intelligence represents a frontier of immense potential, where breakthroughs in materials, device architectures, and quantum phenomena are poised to reshape the landscape of computing. As AI demands continue to grow in complexity, the integration of nanoelectronic technologies offers the promise of dramatically enhancing computational power, energy efficiency, and scalability. From the advent of quantum computing and neuromorphic systems to the development of advanced memory devices like memristors, these innovations offer a tantalizing glimpse into the future of intelligent, adaptive systems capable of tackling challenges once thought insurmountable. However, significant hurdles remain, including issues of scalability, error correction, material heterogeneity, and the seamless integration of quantum, neuromorphic, and classical AI systems. Overcoming these challenges will require sustained interdisciplinary collaboration across the fields of material science, quantum physics, and computational theory, as well as the continued refinement of algorithms tailored to leverage the unique properties of nanoelectronics. Ultimately, the convergence of these technologies will not only drive the next generation of AI applications but also redefine the very nature of computation, enabling intelligent systems that are more powerful, efficient, and versatile than

ever before. As advancements in nanoelectronics and AI continue to accelerate, their integration promises to open new frontiers, redefining the limits of advanced computing and enabling groundbreaking innovations.

References

[1] G. A. Silva, "A new frontier: The convergence of nanotechnology, brain machine interfaces, and artificial intelligence," *Front. Neurosci.*, vol. 12, no. NOV, p. 408236, Nov. 2018, doi: 10.3389/FNINS.2018.00843/BIBTEX.

[2] S. Natale and A. Ballatore, "Imagining the thinking machine: Technological myths and the rise of artificial intelligence," *https://doi.org/10.1177/1354856517715164*, vol. 26, no. 1, pp. 3–18, Jun. 2017, doi: 10.1177/1354856517715164.

[3] Y. Duan, J. S. Edwards, and Y. K. Dwivedi, "Artificial intelligence for decision making in the era of Big Data – evolution, challenges and research agenda," *Int. J. Inf. Manage.*, vol. 48, pp. 63–71, Oct. 2019, doi: 10.1016/J.IJINFOMGT.2019.01.021.

[4] A. Toosi, A. G. Bottino, B. Saboury, E. Siegel, and A. Rahmim, "A Brief History of AI: How to Prevent Another Winter (A Critical Review)," *PET Clin.*, vol. 16, no. 4, pp. 449–469, 2021, doi: 10.1016/j.cpet.2021.07.001.

[5] N. Sharma, R. Sharma, and N. Jindal, "Machine Learning and Deep Learning Applications-A Vision," *Glob. Transitions Proc.*, vol. 2, no. 1, pp. 24–28, Jun. 2021, doi: 10.1016/J.GLTP.2021.01.004.

[6] R. P. Feynman, "There's Plenty of Room at the Bottom," *Caltech Eng. Sci.*, vol. 23, no. 5, pp. 22–36, 1960.

[7] S. Malik, K. Muhammad, and Y. Waheed, "Nanotechnology: A Revolution in Modern Industry," *Molecules*, vol. 28, no. 2, p. 661, Jan. 2023, doi: 10.3390/MOLECULES28020661.

[8] C. Wang, "Nanoelectronics: Materials, Devices and Applications," *Nanomater. 2024, Vol. 14, Page 1716*, vol. 14, no. 21, p. 1716, Oct. 2024, doi: 10.3390/NANO14211716.

[9] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H. S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proc. IEEE*, vol. 89, no. 3, pp. 259–287, 2001, doi: 10.1109/5.915374.

[10] K. S. Novoselov *et al.*, "Electric Field Effect in Atomically Thin Carbon Films," *Science (80-.).*, vol. 306, no. 5696, pp. 666–669, 2004, doi: 10.1126/science.1102896.

[11] P. Prakash, K. Mohana Sundaram, and M. Anto Bennet, "A review on carbon nanotube field effect transistors (CNTFETs) for ultra-low power applications," *Renew. Sustain. Energy Rev.*, vol. 89, pp. 194–203, Jun. 2018, doi: 10.1016/J.RSER.2018.03.021.

[12] B. Anjaneyulu and N. S. S. Reddy, "Design of low power high-speed full, swing 11T CNTFET adder," *e-Prime - Adv. Electr. Eng. Electron. Energy*, vol. 8, p. 100516, Jun. 2024, doi: 10.1016/J.PRIME.2024.100516.

[13] H. Xu, "Signatures of Majorana Fermions in Topological Superconductor Nanowires," 2017, doi: 10.7567/ssdm.2014.p-3-1.

[14] H. J. Levinson, "The potential of EUV lithography," *https://doi.org/10.1117/12.2528446*, vol. 11177, p. 1117702, Aug. 2019, doi: 10.1117/12.2528446.

[15] P. Gargini, F. Balestra, and Y. Hayashi, "Roadmapping of nanoelectronics for the new electronics industry," *Appl. Sci.*, vol. 12, no. 1, 2022, doi: 10.3390/app12010308.

[16] A. Vaswani *et al.*, "Attention is all you need," *Adv. Neural Inf. Process. Syst.*, vol. 2017-Decem, no. Nips, pp. 5999–6009, 2017.

[17] J. Xing *et al.*, "Towards human-like and transhuman perception in," *Front. Inf. Technol. Electron. Eng.*, vol. 18, no. 1, pp. 58–67, 2017.

[18] I. Goodfellow *et al.*, "Generative Adversarial Nets," *Adv. Neural Inf. Process. Syst.*, vol. 27, 2014.

[19] P. Gupta, B. Ding, C. Guan, and D. Ding, "Generative AI: A systematic review using topic modelling techniques," *Data Inf. Manag.*, vol. 8, no. 2, p. 100066, Jun. 2024, doi: 10.1016/J.DIM.2024.100066.

[20] X. Han *et al.*, "Pre-trained models: Past, present and future," *AI Open*, vol. 2, pp. 225–250, 2021, doi: 10.1016/j.aiopen.2021.08.002.

[21] N. P. Jouppi *et al.*, "In-datacenter performance analysis of a tensor processing unit," *Proc. - Int. Symp. Comput. Archit.*, vol. Part F128643, pp. 1–12, Jun. 2017, doi: 10.1145/3079856.3080246.

[22] J. Preskill, "Quantum computing in the NISQ era and beyond," *Quantum*, vol. 2, no. July, pp. 1–20, 2018, doi: 10.22331/q-2018-08-06-79.

[23] D. Patterson *et al.*, "Carbon Emissions and Large Neural Network Training," pp. 1–22, 2021, [Online]. Available: http://arxiv.org/abs/2104.10350

[24] D. Hisamoto, "Historical perspective of the development of the FinFET and process architecture," *75th*

Anniv. Transistor, pp. 145–153, May 2023, doi: 10.1002/9781394202478.CH13.

[25] D. Bhattacharya and N. K. Jha, "FinFETs: From Devices to Architectures," *Adv. Electron.*, vol. 2014, no. 1, p. 365689, Jan. 2014, doi: 10.1155/2014/365689.

[26] R. R. Das, T. R. Rajalekshmi, and A. James, "FinFET to GAA MBCFET: A Review and Insights," *IEEE Access*, vol. 12, no. March, pp. 50556–50577, 2024, doi: 10.1109/ACCESS.2024.3384428.

[27] Q. Zhang, Y. Zhang, Y. Luo, and H. Yin, "New structure transistors for advanced technology node CMOS ICs," *Natl. Sci. Rev.*, vol. 11, no. 3, Feb. 2024, doi: 10.1093/NSR/NWAE008.

[28] R. A. and O. A. M. S. M. S. H. Rafin, "Wide Band Gap Semiconductor Devices for Power Electronic Converters," in *2023 Fourth International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM), Miami, FL, USA*, 2023, pp. 1–8.

[29] M. Srivastava *et al.*, "Recent progress in molybdenum disulfide (MoS2) based flexible nanogenerators: An inclusive review," *Chem. Eng. J.*, vol. 480, p. 147963, Jan. 2024, doi: 10.1016/J.CEJ.2023.147963.

[30] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS2 transistors," *Nat. Nanotechnol.*, vol. 6, no. 3, pp. 147–150, 2011, doi: 10.1038/nnano.2010.279.

[31] G. Indiveri and Y. Sandamirskaya, "The Importance of Space and Time for Signal Processing in Neuromorphic Agents: The Challenge of Developing Low-Power, Autonomous Agents That Interact with the Environment," *IEEE Signal Process. Mag.*, vol. 36, no. 6, pp. 16–28, 2019, doi: 10.1109/MSP.2019.2928376.

[32] M. Prezioso, F. Merrikh-Bayat, B. D. Hoskins, G. C. Adam, K. K. Likharev, and D. B. Strukov, "Training and operation of an integrated neuromorphic network based on metal-oxide memristors," *Nature*, vol. 521, no. 7550, pp. 61–64, 2015, doi: 10.1038/nature14441.

[33] W. T. Navaraj *et al.*, "Nanowire FET based neural element for robotic tactile sensing skin," *Front. Neurosci.*, vol. 11, no. SEP, p. 501, 2017, doi: 10.3389/fnins.2017.00501.

[34] C. Y. Han *et al.*, "An artifical synapse based on graphene field-effect transistor with silver gel/polarized-aptamer gate," *Org. Electron.*, vol. 92, no. December 2020, 2021, doi: 10.1016/j.orgel.2021.106118.

[35] A. Kumar *et al.*, "Optoelectronic memory in 2D MoS2 field effect transistor," *J. Phys. Chem. Solids*, vol. 179, no. April, p. 111406, 2023, doi: 10.1016/j.jpcs.2023.111406.

[36] J. Singh, S. Singh, and N. Paras, "Design and Integration of Vertical TFET and Memristor for Better Realization of Logical Functions," *Silicon*, vol. 15, no. 2, pp. 783–792, Jan. 2023, doi: 10.1007/S12633-022-02047-1/METRICS.

[37] W. C. Chen *et al.*, "Surface ligand engineering of perovskite quantum dots for n-type and stretchable photosynaptic transistor with an ultralow energy consumption," *Chem. Eng. J.*, vol. 494, p. 152897, Aug. 2024, doi: 10.1016/J.CEJ.2024.152897.

[38] J. Puebla, J. Kim, K. Kondou, and Y. Otani, "Spintronic devices for energy-efficient data storage and energy harvesting," *Commun. Mater.*, vol. 1, no. 1, pp. 1–9, 2020, doi: 10.1038/s43246-020-0022-5.

[39] M. Rostami and K. Mohanram, "Dual-Vth independent-gate FinFETs for low power logic circuits," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 30, no. 3, pp. 337–349, Mar. 2011, doi: 10.1109/TCAD.2010.2097310.

[40] [40] E. D. Kurniawan, H. Yang, C. C. Lin, and Y. C. Wu, "Effect of fin shape of tapered FinFETs on the device performance in 5-nm node CMOS technology," *Microelectron. Reliab.*, vol. 83, pp. 254–259, 2018, doi: 10.1016/j.microrel.2017.06.037.

[41] Q. Zhang, Y. Zhang, Y. Luo, and H. Yin, "New structure transistors for advanced technology node CMOS ICs," *Natl. Sci. Rev.*, vol. 11, no. 3, 2024, doi: 10.1093/nsr/nwae008.

[42] T. Shan, "Advantages of FINFET over traditional CMOS: Reasons and implications," *Theor. Nat. Sci.*, vol. 14, no. 1, pp. 219–223, Nov. 2023, doi: 10.54254/2753-8818/14/20241010.

[43] A. B. A. Tahrim, H. C. Chin, C. S. Lim, and M. L. P. Tan, "Design and performance analysis of 1-Bit FinFET full adder cells for subthreshold region at 16 nm process technology," *J. Nanomater.*, vol. 2015, 2015, doi: 10.1155/2015/726175.

[44] K. I. Seo *et al.*, "A 10nm platform technology for low power and high performance application featuring FINFET devices with multi workfunction gate stack on bulk and SOI," *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. 5–6, 2014, doi: 10.1109/VLSIT.2014.6894342.

[45] J. Ajayan *et al.*, "Nanosheet field effect transistors-A next generation device to keep Moore's law alive: An intensive study," *Microelectronics J.*, vol. 114, no. June, p. 105141, 2021, doi: 10.1016/j.mejo.2021.105141.

[46] U. K. Das and T. K. Bhattacharyya, "Opportunities in Device Scaling for 3-nm Node and Beyond: FinFET Versus GAA-FET Versus UFET," *IEEE Trans. Electron Devices*, vol. 67, no. 6, pp. 2633–2638, Jun. 2020, doi: 10.1109/TED.2020.2987139.

[47] S. Kim *et al.*, "Investigation of Device Performance for Fin Angle Optimization in FinFET and Gate-All-Around FETs for 3 nm-Node and Beyond," *IEEE Trans. Electron Devices*, vol. 69, no. 4, pp. 2088–2093, Apr. 2022, doi: 10.1109/TED.2022.3154683.

[48] A. Veloso, P. Matagne, D. Jang, G. Eneman, N. Horiguchi, and J. Ryckaert, "Nanowire & Nanosheet FETs for Ultra-Scaled, High-Density Logic and Memory Applications," *Solid State Electron.*, p. 107736, 2019, doi: 10.1016/j.sse.2019.107736.

[49] J. Z. Sagarika Mukesh, "A Review of the Gate-All-Around Nanosheet FET," *Electronics*, vol. 11, no. 21, p. 3589, 2022, doi: https://doi.org/10.3390/electronics11213589.

[50] G. Bae *et al.*, "3nm GAA Technology featuring Multi-Bridge-Channel FET for Low Power and High Performance Applications," *2018 IEEE Int. Electron Devices Meet.*, pp. 28.7.1-28.7.4, 2018.

[51] H. Wong and K. Kakushima, "On the Vertically Stacked Gate-All-Around Nanosheet and Nanowire Transistor Scaling beyond the 5 nm Technology Node," pp. 1–15, 2022.

[52] "3nm Technology - Taiwan Semiconductor Manufacturing Company Limited." Accessed: Nov. 20, 2024. [Online]. Available: https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_3nm

[53] N. Collaert, "From FinFET to Nanosheets and Beyond," in *Springer Handbook of Semiconductor Devices . Springer Handbooks. Springer*, R. Rudan, M., Brunetti, R., Ed., 2023, pp. 259–278.

[54] O. Sikder and P. J. Schubert, "First Principle and NEGF Based Study of Silicon Nano-wire and Nano-sheet for Next Generation FETs: Performance, Interface Effects and Lifetime," *Proc. IEEE Conf. Nanotechnol.*, vol. 2020-July, pp. 140–145, Jul. 2020, doi: 10.1109/NANO47656.2020.9183675.

[55] B. Kim, S. Lee, and J. H. Park, "Innovations of metallic contacts on semiconducting 2D transition metal dichalcogenides toward advanced 3D-structured field-effect transistors," *Nanoscale Horizons*, vol. 9, no. 9, pp. 1417–1431, Aug. 2024, doi: 10.1039/D4NH00030G.

[56] S. Jung *et al.*, "A crossbar array of magnetoresistive memory devices for in-memory computing," *Nat. 2022 6017892*, vol. 601, no. 7892, pp. 211–216, Jan. 2022, doi: 10.1038/s41586-021-04196-6.

[57] H. S. P. Wong *et al.*, "Recent progress of phase change memory (PCM) and resistive switching random access memory (RRAM)," *ICSICT-2010 - 2010 10th IEEE Int. Conf. Solid-State Integr. Circuit Technol. Proc.*, pp. 1055–1060, 2010, doi: 10.1109/ICSICT.2010.5667542.

[58] G. W. Burr *et al.*, "Neuromorphic computing using non-volatile memory," *Adv. Phys. X*, vol. 2, no. 1, pp. 89–124, 2017, doi: 10.1080/23746149.2016.1259585.

[59] S. Gupta, A. Agrawal, K. Gopalakrishnan, and P. Narayanan, "Deep learning with limited numerical precision," *32nd Int. Conf. Mach. Learn. ICML 2015*, vol. 3, pp. 1737–1746, 2015.

[60] H. S. P. Wong *et al.*, "Metal-oxide RRAM," *Proc. IEEE*, vol. 100, no. 6, pp. 1951–1970, 2012, doi: 10.1109/JPROC.2012.2190369.

[61] Q. Zhang, M. Zhang, T. Chen, Z. Sun, Y. Ma, and B. Yu, "Recent advances in convolutional neural network acceleration," *Neurocomputing*, vol. 323, pp. 37–51, 2019, doi: 10.1016/j.neucom.2018.09.038.

[62] A. D. Kent and D. C. Worledge, "A new spin on magnetic memories," *Nat. Nanotechnol.*, vol. 10, no. 3, pp. 187–191, 2015, doi: 10.1038/nnano.2015.24.

[63] D. Apalkov *et al.*, "Spin-transfer torque magnetic random access memory (STT-MRAM)," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 9, no. 2, pp. 1–35, 2013, doi: 10.1145/2463585.2463589.

[64] S. Ambrogio *et al.*, "Equivalent-accuracy accelerated neural-network training using analogue memory," *Nat. 2018 5587708*, vol. 558, no. 7708, pp. 60–67, Jun. 2018, doi: 10.1038/s41586-018-0180-5.

[65] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nat. 2008 4537191*, vol. 453, no. 7191, pp. 80–83, May 2008, doi: 10.1038/nature06932.

[66] J. J. Yang, D. B. Strukov, and D. R. Stewart, "Memristive devices for computing," *Nat. Nanotechnol.*, vol. 8, no. 1, pp. 13–24, 2013, doi: 10.1038/nnano.2012.240.

[67] C. Li *et al.*, "Analogue signal and image processing with large memristor crossbars," *Nat. Electron.*, vol. 1, no. 1, pp. 52–59, 2018, doi: 10.1038/s41928-017-0002-z.

[68] G. Indiveri and S. C. Liu, "Memory and Information Processing in Neuromorphic Systems," *Proc. IEEE*, vol. 103, no. 8, pp. 1379–1397, Aug. 2015, doi: 10.1109/JPROC.2015.2444094.

[69] Y. Zhang, Z. Jia, H. Du, R. Xue, Z. Shen, and Z. Shao, "A Practical Highly Paralleled ReRAM-Based DNN Accelerator by Reusing Weight Pattern Repetitions," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 41, no. 4, pp. 922–935, Apr. 2022, doi: 10.1109/TCAD.2021.3071116.

[70] P. A. Merolla *et al.*, "A million spiking-neuron integrated circuit with a scalable communication network and interface," *Science (80-.).*, vol. 345, no. 6197, pp. 668–673, 2014, doi: 10.1126/science.1254642.

[71] M. Davies *et al.*, "Loihi: A Neuromorphic Manycore Processor with On-Chip Learning," *IEEE Micro*, vol. 38, no. 1, pp. 82–99, 2018, doi: 10.1109/MM.2018.112130359.

[72] [72] B. S. Panisello, "Spiking Neural Networks - Models and Implementations : Exploring spiking neural network models and implementations for simulating biological neural networks and brain-inspired computing," vol. 3, no. 2, pp. 292–303.

[73] [73] C. D. Schuman, S. R. Kulkarni, M. Parsa, J. P. Mitchell, P. Date, and B. Kay, "Opportunities for neuromorphic computing algorithms and applications," *Nat. Comput. Sci. 2022 21*, vol. 2, no. 1, pp. 10–19, Jan. 2022, doi: 10.1038/s43588-021-00184-y.

[74] S. J. Kim, S. B. Kim, and H. W. Jang, "Competing memristors for brain-inspired computing," *iScience*,

vol. 24, no. 1, p. 101889, Jan. 2021, doi: 10.1016/J.ISCI.2020.101889.

[75] H. Seok, S. Son, S. B. Jathar, J. Lee, and T. Kim, "Synapse-Mimetic Hardware-Implemented Resistive Random-Access Memory for Artificial Neural Network," *Sensors*, vol. 23, no. 6, 2023, doi: 10.3390/s23063118.

[76] I. Muñoz-Martin, S. Bianchi, S. Hashemkhani, G. Pedretti, O. Melnic, and D. Ielmini, "A Brain-Inspired Homeostatic Neuron Based on Phase-Change Memories for Efficient Neuromorphic Computing," *Front. Neurosci.*, vol. 15, p. 709053, Aug. 2021, doi: 10.3389/FNINS.2021.709053/BIBTEX.

[77] S. Wang *et al.*, "Memristor-Based Intelligent Human-Like Neural Computing," *Adv. Electron. Mater.*, vol. 9, no. 1, p. 2200877, Jan. 2023, doi: 10.1002/AELM.202200877.

[78] Y. Lv, H. Chen, Q. Wang, X. Li, C. Xie, and Z. Song, "Post-silicon nano-electronic device and its application in brain-inspired chips," *Front. Neurorobot.*, vol. 16, p. 948386, Jul. 2022, doi: 10.3389/FNBOT.2022.948386.

[79] H. Paugam-Moisy and S. Bohte, "Computing with Spiking Neuron Networks," *Handb. Nat. Comput.*, vol. 1–4, pp. 335–376, Jan. 2012, doi: 10.1007/978-3-540-92910-9_10.

[80] N. Kasabov, K. Dhoble, N. Nuntalid, and G. Indiveri, "Dynamic evolving spiking neural networks for on-line spatio- and spectro-temporal pattern recognition," *Neural Networks*, vol. 41, pp. 188–201, May 2013, doi: 10.1016/J.NEUNET.2012.11.014.

[81] W. Guo, M. E. Fouda, A. M. Eltawil, and K. N. Salama, "Neural Coding in Spiking Neural Networks: A Comparative Study for Robust Neuromorphic Systems," *Front. Neurosci.*, vol. 15, no. March, pp. 1–21, 2021, doi: 10.3389/fnins.2021.638474.

[82] S. Jiang, S. Nie, Y. He, R. Liu, C. Chen, and Q. Wan, "Emerging synaptic devices: from two-terminal memristors to multiterminal neuromorphic transistors," *Mater. Today Nano*, vol. 8, Dec. 2019, doi: 10.1016/j.mtnano.2019.100059.

[83] D. Gerlinghoff, T. Luo, R. S. M. Goh, and W. F. Wong, "Desire backpropagation: A lightweight training algorithm for multi-layer spiking neural networks based on spike-timing-dependent plasticity," *Neurocomputing*, vol. 560, pp. 1–16, 2023, doi: 10.1016/j.neucom.2023.126773.

[84] Z. Bing, I. Baumann, Z. Jiang, K. Huang, C. Cai, and A. Knoll, "Supervised learning in SNN via reward-modulated spike-timing-dependent plasticity for a target reaching vehicle," *Front. Neurorobot.*, vol. 13, p. 438145, May 2019, doi: 10.3389/FNBOT.2019.00018/BIBTEX.

[85] C. Hughes, J. Isaacson, A. Perry, R. F. Sun, and J. Turner, "Quantum Gates," *Quantum Comput. Quantum Curious*, pp. 49–57, 2021, doi: 10.1007/978-3-030-61601-4_6.

[86] A. Sigov, L. Ratkin, and L. A. Ivanov, "Quantum Information Technology," *J. Ind. Inf. Integr.*, vol. 28, p. 100365, Jul. 2022, doi: 10.1016/J.JII.2022.100365.

[87] A. Cicero, M. A. Maleki, M. W. Azhar, A. F. Kockum, and P. Trancoso, "Simulation of Quantum Computers: Review and Acceleration Opportunities," Oct. 2024, Accessed: Nov. 14, 2024. [Online]. Available: https://arxiv.org/abs/2410.12660v1

[88] M. Veldhorst, H. G. J. Eenink, C. H. Yang, and A. S. Dzurak, "Silicon CMOS architecture for a spin-based quantum computer," *Nat. Commun.*, vol. 8, no. 1, 2017, doi: 10.1038/s41467-017-01905-6.

[89] M. R. Khan, H. Khan, I. Alam, and S. T. Siddiqui, "Analysis and Implementation of Quantum Gates (X , Z , Y , Hadamard CNOT and CCNOT) by using matrices for Quantum Computing," vol. 32, no. 1, pp. 507–520, 2025.

[90] Y. Liao, M. H. Hsieh, and C. Ferrie, "Quantum optimization for training quantum neural networks," *Quantum Mach. Intell.*, vol. 6, no. 1, pp. 1–29, Jun. 2024, doi: 10.1007/S42484-024-00169-W/FIGURES/30.

[91] T. Suzuki, T. Hasebe, and T. Miyazaki, "Quantum support vector machines for classification and regression on a trapped-ion quantum computer," *Quantum Mach. Intell.*, vol. 6, no. 1, pp. 1–14, 2024, doi: 10.1007/s42484-024-00165-0.

[92] A. G. Fowler, M. Mariantoni, J. M. Martinis, and A. N. Cleland, "Surface codes: Towards practical large-scale quantum computation," *Phys. Rev. A - At. Mol. Opt. Phys.*, vol. 86, no. 3, 2012, doi: 10.1103/PhysRevA.86.032324.

[93] J. T. Fourkas *et al.*, "Grand Challenges in Nanofabrication: There Remains Plenty of Room at the Bottom," *Front. Nanotechnol.*, vol. 3, no. October, pp. 2–5, 2021, doi: 10.3389/fnano.2021.700849.

[94] X. You, Z. Huang, U. Alyanak, A. Romanenko, A. Grassellino, and S. Zhu, "Stabilizing and Improving Qubit Coherence by Engineering the Noise Spectrum of Two-Level Systems," *Phys. Rev. Appl.*, vol. 18, no. 4, p. 044026, Oct. 2022, doi: 10.1103/PHYSREVAPPLIED.18.044026/FIGURES/7/MEDIUM.

[95] Z. Zhang, X. Wang, and Y. Yan, "A review of the state-of-the-art in electronic cooling," *e-Prime - Adv. Electr. Eng. Electron. Energy*, vol. 1, p. 100009, Jan. 2021, doi: 10.1016/J.PRIME.2021.100009.

[96] K. Sathish, A. Sathya, P. Pattunnarajam, A. S. Rao, S. Lakshmisridevi, and C. Pushpa Priya, "Innovative Approaches in Advanced VLSI Design for High-Performance Computing Applications," *2nd Int. Conf. Intell. Cyber Phys. Syst. Internet Things, ICoICI 2024 - Proc.*, pp. 643–648, 2024, doi:

10.1109/ICOICI62503.2024.10696557.

[97]   J. Levy, "Correlated nanoelectronics and the second quantum revolution," *APL Mater.*, vol. 10, no. 11, Nov. 2022, doi: 10.1063/5.0111221/20038016/110901_1_5.0111221.AM.PDF.

[98]   J. R. McClean, J. Romero, R. Babbush, and A. Aspuru-Guzik, "The theory of variational hybrid quantum-classical algorithms," *New J. Phys.*, vol. 18, no. 2, p. 023023, Feb. 2016, doi: 10.1088/1367-2630/18/2/023023.

[99]   K. Blekos *et al.*, "A review on Quantum Approximate Optimization Algorithm and its variants," *Phys. Rep.*, vol. 1068, pp. 1–66, Jun. 2024, doi: 10.1016/J.PHYSREP.2024.03.002.

[100]   M. Shahsavari, D. Thomas, M. van Gerven, A. Brown, and W. Luk, "Advancements in spiking neural network communication and synchronization techniques for event-driven neuromorphic systems," *Array*, vol. 20, p. 100323, Dec. 2023, doi: 10.1016/J.ARRAY.2023.100323.

[101]   K. Sun, J. Chen, and X. Yan, "The Future of Memristors: Materials Engineering and Neural Networks," *Adv. Funct. Mater.*, vol. 31, no. 8, p. 2006773, Feb. 2021, doi: 10.1002/ADFM.202006773.

[102]   L. Ye *et al.*, "Overview of Memristor-Based Neural Network Design and Applications," *Front. Phys.*, vol. 10, p. 839243, Jul. 2022, doi: 10.3389/FPHY.2022.839243/BIBTEX.

[103]   D. Marković, A. Mizrahi, D. Querlioz, and J. Grollier, "Physics for neuromorphic computing," *Nat. Rev. Phys.*, vol. 2, no. 9, pp. 499–510, 2020, doi: 10.1038/s42254-020-0208-2.