

Performance and Design Optimisation of 7TRAM Cell Based on Dynamic Thresholds

Rajender Kumar¹, Dayanand Dev²

¹Assistant Professor, Electronics and Communication Engineering Department, NIT Kurukshetra, India.

²M. Tech Student, Electronics and Communication Engineering Department, NIT Kurukshetra, India.

As technology scales down to nanometer regimes, such as 90 nm and below, leakage power becomes a dominant component of total power dissipation in SRAM cells. This increased power consumption poses a challenge for battery-operated and portable devices, where power efficiency is critical. Additionally, high power dissipation can lead to thermal issues, impacting the reliability and longevity of electronic devices. The comparative analysis highlighted that the DTMOS with Sleep technique offers the best balance between power dissipation and propagation delay. The Stack with Sleep technique provides the greatest power savings but at the cost of increased delay, making it suitable for ultra-low-power applications where speed is less critical. This paper demonstrated the effectiveness of various low-power techniques in the design of 7T SRAM cells. The combination of variable threshold and sleep transistors emerged as the most promising approach, offering significant power savings with minimal impact on performance.

Keywords: SRAM cells, power dissipation, propagation delay, Energy Delay Product (EDP).

1. Introduction

1.1 Background

Static Random-Access Memory (SRAM) is a type of semiconductor memory widely used in various electronic devices for its high speed and low power consumption characteristics. SRAM cells, due to their volatile nature, retain data only when the power supply is active, making them crucial for applications that require fast and efficient memory access such as caches in microprocessors, mobile devices, and other high-performance computing systems.

The traditional 6-transistor (6T) SRAM cell is commonly used due to its simplicity and reliability. However, with the continuous scaling of technology nodes, the leakage power of SRAM cells has become a significant concern. Leakage power, which is the power consumed by the transistor when it is in an off state, becomes more pronounced as transistors shrink in size.

1.2 Problem Statement

To address these challenges, various low-power techniques have been proposed to reduce leakage power in SRAM cells. This paper focuses on the design and comparative analysis of a 7-transistor (7T) SRAM cell incorporating several low-power techniques: sleep transistor, variable threshold (VT), transistor stacking, VT with sleep transistor, and stack transistor with sleep transistor. Each technique offers unique benefits in reducing power dissipation and enhancing the overall performance of SRAM cells.

1.3 Objectives

The primary objectives of this paper are:

1. **Designing 7T SRAM Cells:** Implement the baseline 7T SRAM cell using conventional MOSFETs and then integrate the proposed low-power techniques.
2. **Simulation and Analysis:** Perform detailed simulations using the 90 nm Predictive Technology Model (PTM) in LTSpiceXVII software to evaluate the performance of each design.
3. **Performance Metrics Evaluation:** Analyze key performance metrics, including power dissipation, propagation delay, Power Delay Product (PDP), and Energy Delay Product (EDP).
4. **Comparative Study:** Conduct a comparative study to determine the most effective low-power technique for 7T SRAM cells in terms of power efficiency and performance.

1.4 Scope of the Paper

The scope of this paper includes:

- Designing and simulating 7T SRAM cells using five different low-power techniques.
- Evaluating the impact of these techniques on power dissipation and propagation delay.
- Comparing the results with conventional MOSFET-based 7T SRAM cells to determine the improvements achieved.

This paper does not cover:

- The fabrication of the designed SRAM cells.
- The impact of these techniques on other parameters such as noise margins and cell stability, which could be potential areas for future research.

1.5 Organization of the Paper

The paper is organized as follows:

- **Literature Review:** Discusses previous research and existing techniques for reducing power consumption in SRAM cells.
- **Methodology:** Details the tools, technology, and performance metrics used in the simulation and analysis of the SRAM designs.
- **Design Techniques:** Describes the implementation and mathematical analysis of each low-power technique applied to the 7T SRAM cells.

- **Simulation and Results:** Presents the simulation results for each design technique, including power dissipation and propagation delay.
- **Comparative Analysis:** Compares the performance of the different low-power techniques and discusses their effectiveness.
- **Conclusion and Future Work:** Summarizes the findings of the paper and suggests directions for future research.
- **References:** Lists the sources referenced throughout the paper.

2. Objectives

- To reduce dynamic and static power dissipation in 7T SRAM cells.
- To evaluate the effectiveness of Variable Threshold CMOS, Sleep Transistor, and Transistor Stacking techniques.
- To compare the power consumption of the optimized 7T SRAM with conventional designs.

3. Methodology

The paper follows a structured approach to design, simulate, and analyze 7T SRAM cells using the aforementioned low-power techniques.

3.1 Tools and Technology

- **Technology Node:** 90 nm Predictive Technology Model (PTM)
- **Simulation Software:** LTSpiceXVII
- **Supply Voltage (Vdd):** 300 mV

3.2 Performance Metrics

- **Power Dissipation:** The total power consumed by the SRAM cell during operation.
- **Propagation Delay:** The time taken for a signal to propagate through the SRAM cell.
- **Power Delay Product (PDP):** The product of power dissipation and propagation delay, indicating overall efficiency.

$$PDP = P \times t_{pd}$$

- **Energy Delay Product (EDP):** The product of energy consumed and delay, providing a comprehensive measure of performance.

$$EDP = E \times t_{pd} = P \times t_{pd}^2$$

4. Design Techniques

4.1 Basic 7T SRAM Cell

The 7T SRAM cell configuration shown in Fig.1, is an enhanced version of the traditional 6T SRAM cell. The primary difference lies in the addition of an extra NMOS transistor in the ground path of the cross-coupled inverters that form the core of the SRAM cell. This additional transistor helps to reduce voltage leakage during the read operation by cutting off the ground path, thereby improving the cell's stability and performance.

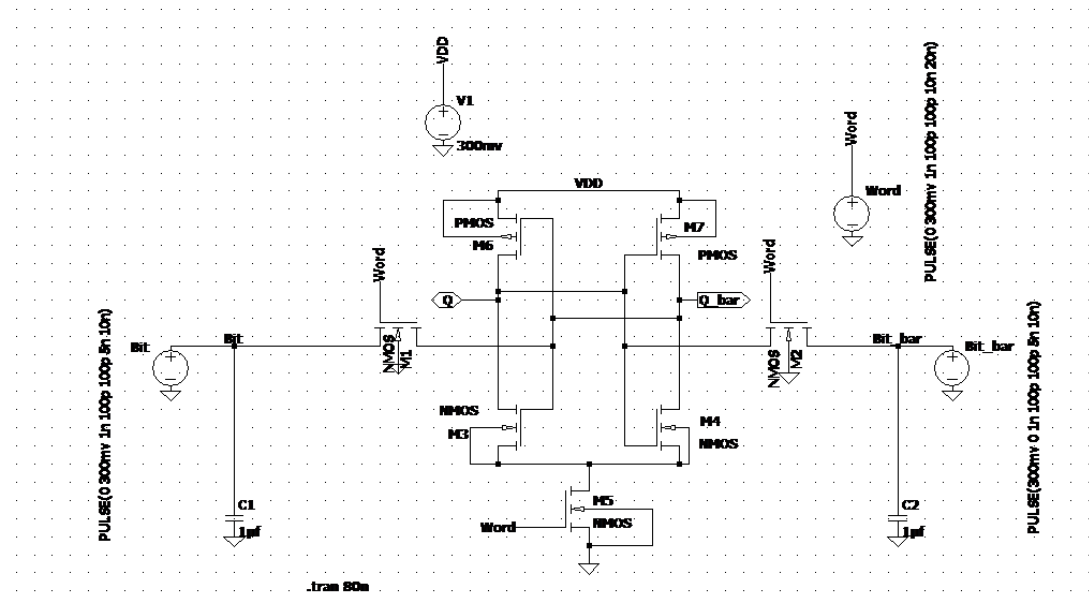


Fig. 1. Schematic of 7T SRAM Cell.

Key Components of the 7T SRAM Cell

1. Cross-Coupled Inverters (M3 and M4):
 - These transistors form the core memory storage elements. They are responsible for holding the logic state (either 0 or 1) at nodes Q and Q bar.
2. Access Transistors (M1 and M2):
 - These NMOS transistors control access to the cell for read and write operations. They connect the internal nodes (Q and Q bar) to the bit lines (BL and BLB) when the word line (WL) is activated.
3. Bit Lines (BL and BLB):
 - BL and BLB are used to transfer data to and from the SRAM cell during write and read operations. BL is typically connected to the drain of M1, and BLB is connected to the drain of M2.

4. Word Line (WL):

- The word line is used to select a specific SRAM cell for read or write operations. When the WL is high, it activates the access transistors (M1 and M2), allowing data to be written to or read from the cell.

5. Additional NMOS Transistor:

- This transistor is connected in series with the ground path of the cross-coupled inverters. During the read operation, it helps to isolate the cell from the ground, thereby preventing voltage leakage from node Q to ground.

Operation of the 7T SRAM Cell

Write Operation:

- When the word line (WL) is high, both access transistors (M1 and M2) turn on.
- Data is written to the cell through the bit lines (BL and BLB). For instance, if a logic '1' is to be written:
- BL is driven high.
- BLB is driven low.
- The cross-coupled inverters (M3 and M4) latch the new data, storing the logic '1' at node Q and logic '0' at node Q bar.

Read Operation:

- The word line (WL) is activated, turning on the access transistors (M1 and M2).
- The state of the cell is sensed by the bit lines. For example, if Q is high and Q bar is low:
- BL will sense a high voltage.
- BLB will sense a low voltage.
- The additional NMOS transistor in the ground path is turned off during this operation to prevent voltage leakage from Q to ground, thereby maintaining the integrity of the stored data.

Advantages of the 7T SRAM Cell

- **Reduced Leakage:** The additional NMOS transistor effectively reduces voltage leakage during the read operation, which enhances data stability.
- **Improved Performance:** By isolating the ground path during reads, the cell can achieve better performance and reliability compared to the traditional 6T SRAM cell.

4.2 Sleep Transistor

Sleep transistors are used to disconnect the SRAM cell from the power supply during idle periods, significantly reducing static power dissipation as shown in Fig.2.

Key Concepts in Power Gating and Sleep Transistors

1. Sleep Transistors:

- Sleep transistors are high threshold voltage transistors that are used to disconnect the circuit from the power supply during standby mode, thereby reducing leakage currents.
- They create what is known as a "virtual power supply" and a "virtual ground," effectively isolating the circuit when it is not in use.

2. Virtual Power Supply and Ground:

- The virtual power supply (connected to VDD through a PMOS sleep transistor) and virtual ground (connected to VSS through an NMOS sleep transistor) are essential components in power gating.
- This arrangement helps in integrating the devices and reducing leakage currents by turning off the sleep transistors during standby modes.

3. Header and Footer Switches:

- The PMOS sleep transistor, referred to as the "header switch," is used to control the connection to the power supply (VDD).
- The NMOS sleep transistor, referred to as the "footer switch," controls the connection to the ground (VSS).
- These switches ensure that the circuit can be completely isolated from both power supply and ground during standby, effectively cutting off leakage paths.

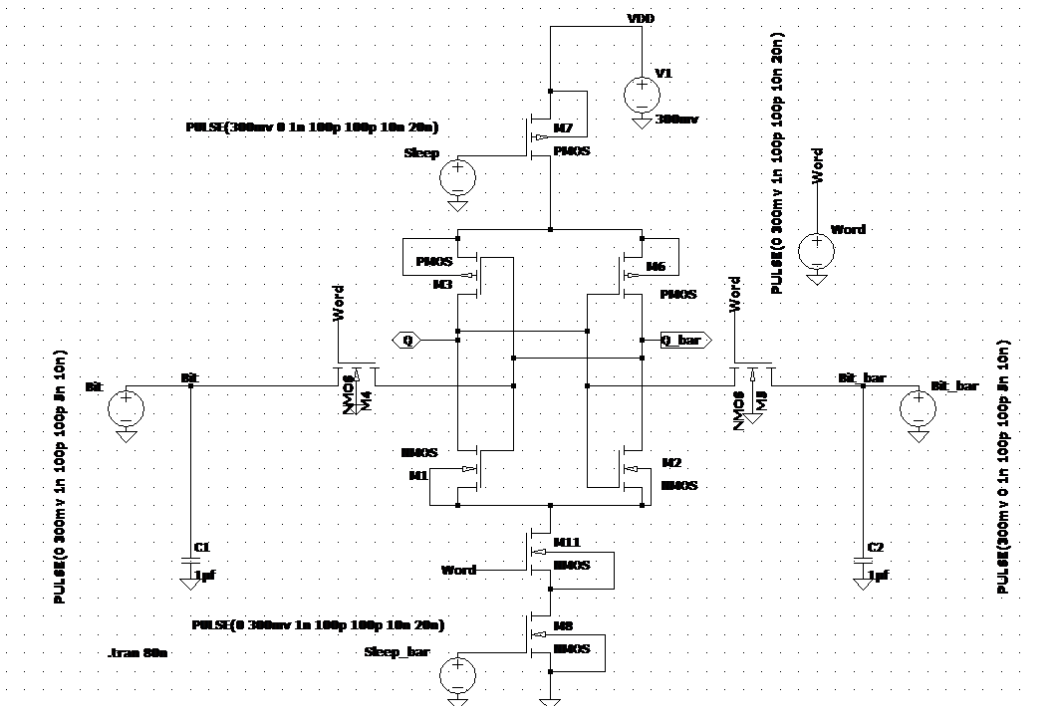


Fig. 2. Schematic of SRAM cell with Sleep Transistor Technique

4. Operation of Sleep Transistors:

- During active operation, the sleep transistors are turned on, connecting the circuit to the power supply and ground, and allowing normal operation.
- During standby mode, the sleep transistors are turned off. This isolates the circuit, thereby reducing leakage currents significantly.
- Specifically, when an NMOS transistor is used as a sleep transistor on the pull-down path, a SLEEP signal is generated to control its state. When the circuit is in standby, this transistor is turned off, making the gate terminal of the transistor float and cutting off the leakage path.

4.3 Dynamic threshold MOSFET (DTMOS)

Adjusts the threshold voltage dynamically based on the operational state to improve drive current and reduce leakage power.

In a DTMOS (Dynamic Threshold MOSFET) as shown in Fig.3, the body and gate terminals are connected, introducing a body effect. This dynamic connection causes the threshold voltages of NMOS and PMOS transistors to change in response to variations in the gate voltage. When the gate voltage is zero, the DTMOS behaves similarly to a conventional MOSFET.

- Use body biasing or back-gate control to change the threshold voltage of the transistors.
- Apply a higher threshold voltage during idle periods and a lower threshold during active periods.

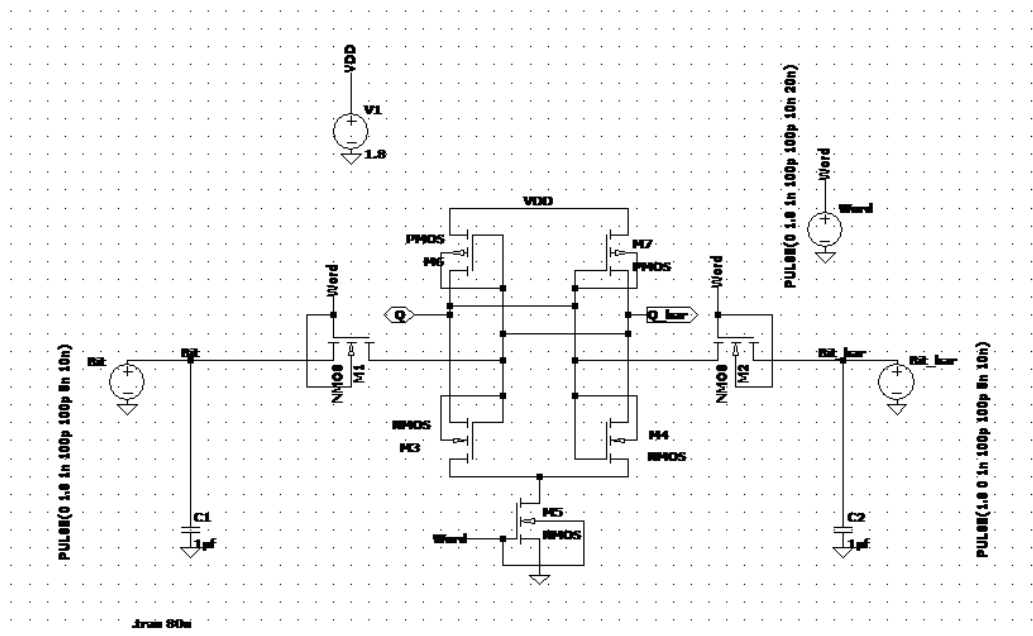


Fig. 3. Schematic of SRAM using DTMOS Technique.

4.4 Transistor Stacking

Stacking transistors in series reduces leakage current through sub-threshold leakage reduction. The transistor stacking technique is a well-known method for reducing leakage power in CMOS circuits. By arranging multiple transistors in series, this technique increases the effective threshold voltage, thereby reducing sub-threshold leakage currents. This method is particularly effective in standby modes where leakage power is a significant concern.

Implementation:

- Replace single transistors with series-connected transistors in the pull-up and pull-down networks of the SRAM cell as shown in Fig.4.
- Increased Effective Threshold Voltage (V_{th})
- Reduced Drain-Source Voltage (V_{ds})
- In a stacked configuration, the voltage across each transistor (V_{ds}) is lower, which also reduces the sub-threshold leakage current. This occurs because the voltage drop is shared among the transistors in the stack.

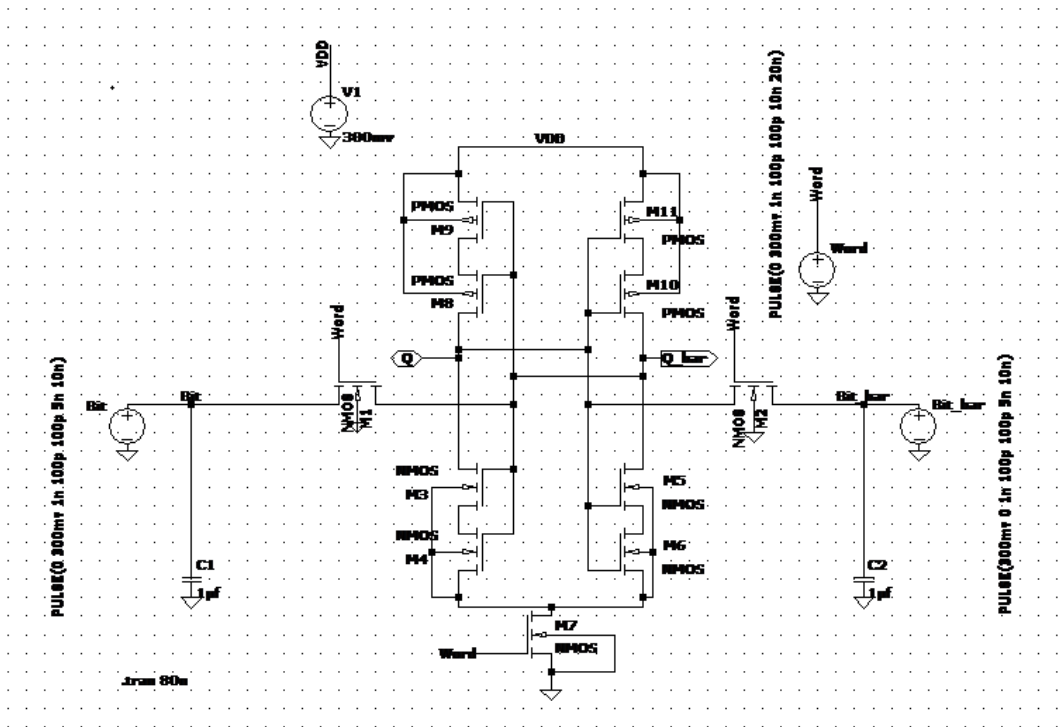


Fig. 4. Schematic of SRAM using Transistor Stacking Technique

4.5 Dynamic threshold MOSFET (DTMOS) with Sleep Transistor.

Description: Combines the benefits of variable threshold adjustment and sleep transistors to achieve better power savings.

Implementation:

- Integrate both DT MOS and sleep transistor techniques into the SRAM cell design as shown in Fig.5.
- 7T SRAM cell with both body-bias control and sleep transistors.

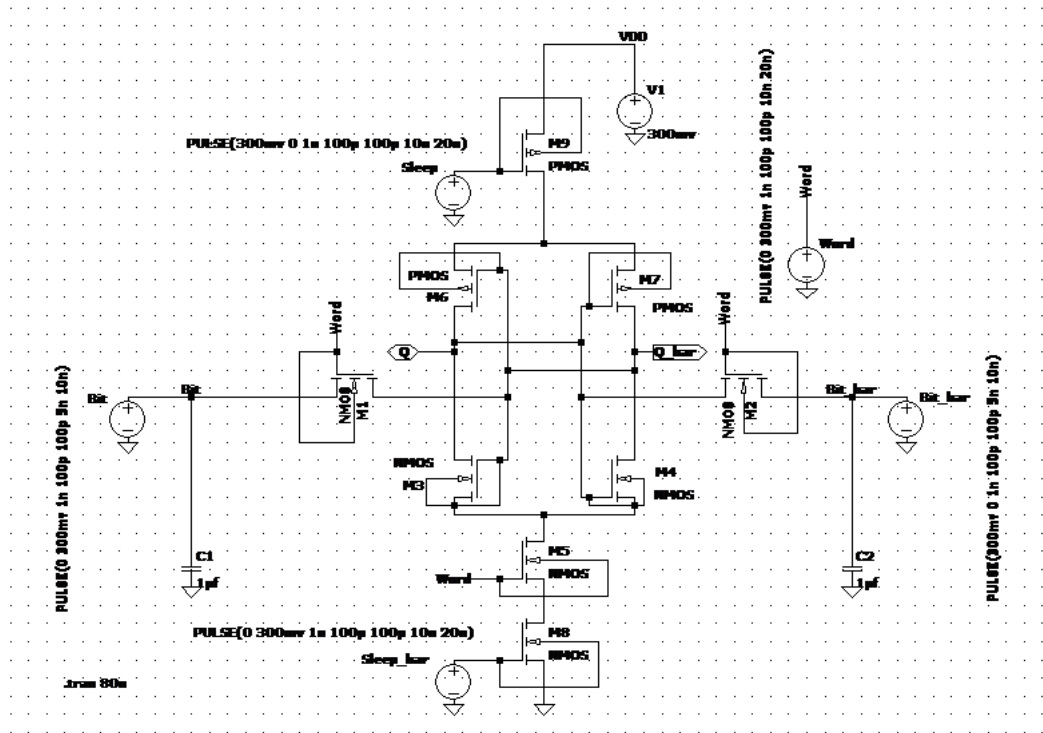


Fig. 5. Schematic of 7T DT MOS SRAM Cell with Sleep Transistor Technique.

4.6 Stack Transistor with Sleep Transistor

Description: Utilizes both transistor stacking and sleep transistors to minimize power dissipation while maintaining performance.

Implementation:

- Combine series-connected transistors (stacking) with sleep transistors in the SRAM cell.
- 7T SRAM cell with series-connected transistors and sleep transistor as shown in Fig.6.

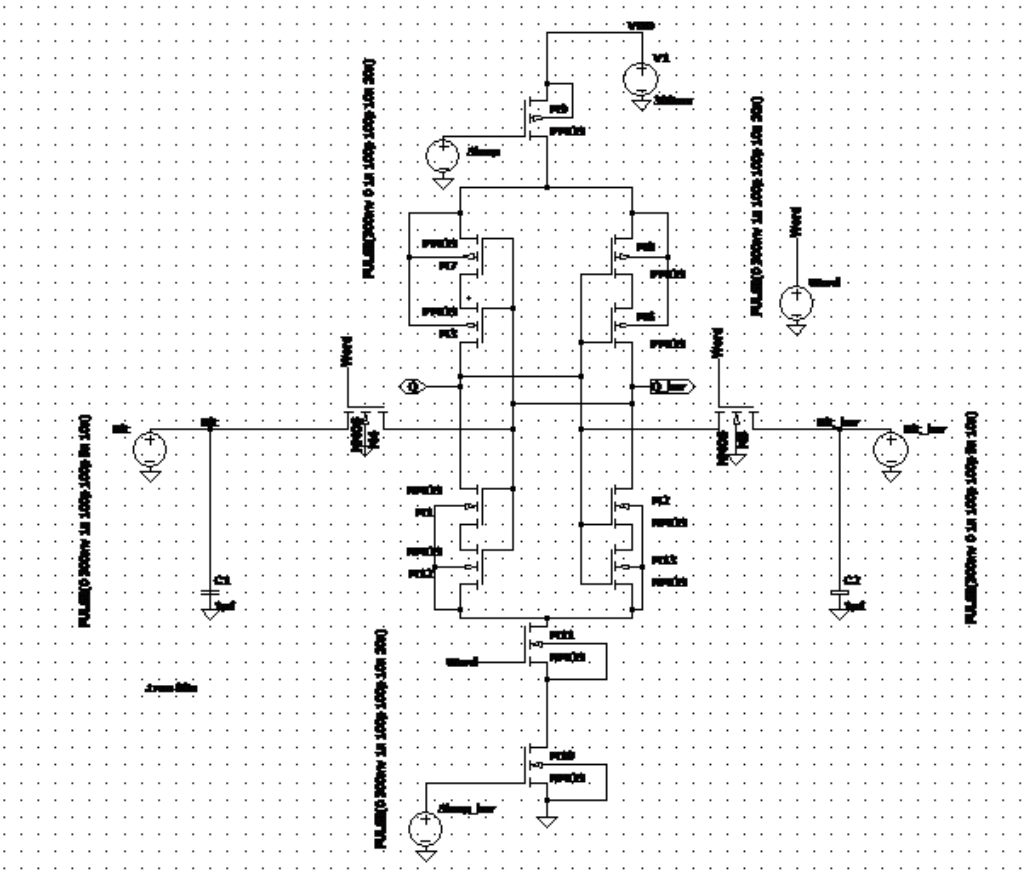


Fig. 6. Schematic of 7T SRAM Cell with Stacking & Sleep Transistor Technique.

5. Simulation and Results

Simulations were conducted for each design technique, and the following results were recorded:

5.1 Power Dissipation and Delay of Basic 7T SRAM

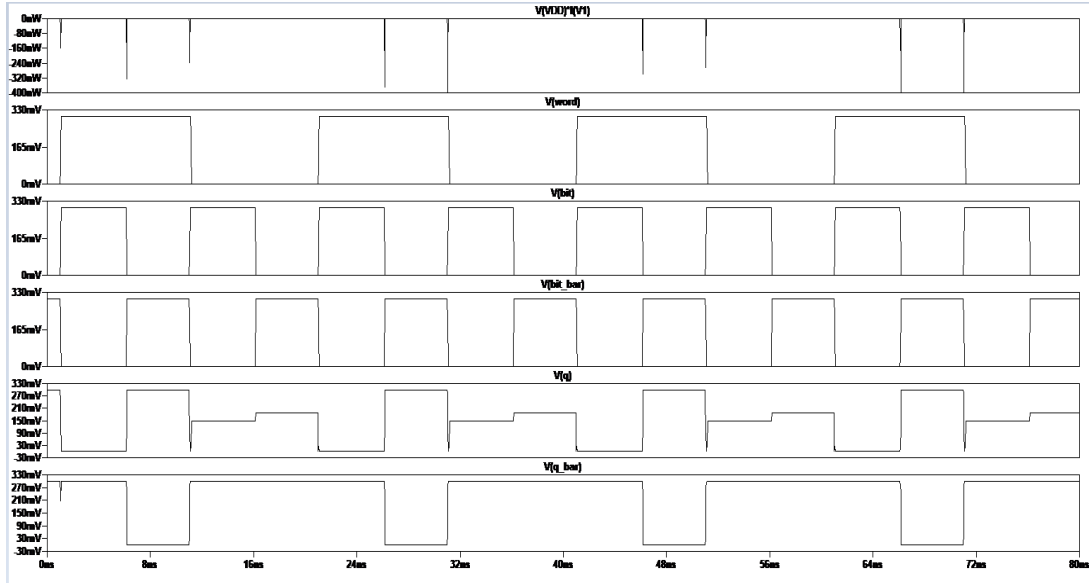


Fig.7 Waveforms of 7T conventional MOSFET cell.

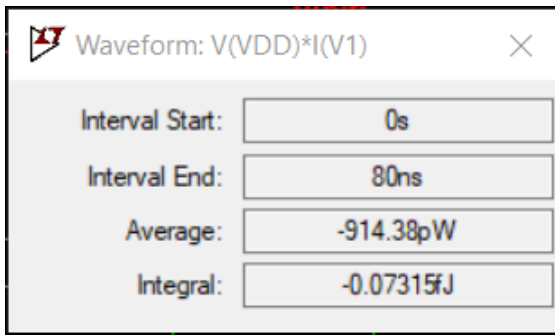


Fig. 8 Average Power

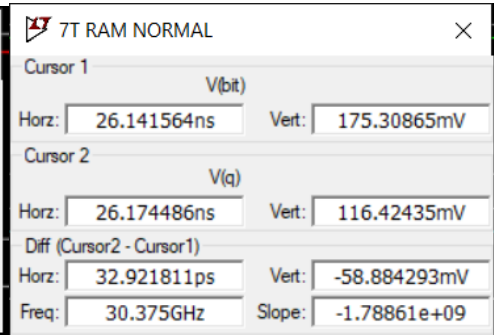


Fig.9 Delay

- Power Delay Product (PDP): The product of power dissipation and propagation delay, indicating overall efficiency.

$$PDP = P \times t_{pd} = 301.023 \times 10^{-22} \text{ W} \cdot \text{Sec (Joule)}$$

- Energy Delay Product (EDP): The product of energy consumed and delay, providing a comprehensive measure of performance.

$$EDP = E \times t_{pd} = P \times t_{pd}^2 = 99.099 \times 10^{-32} \text{ J} \cdot \text{Sec}$$

5.2 Power Dissipation and Delay of 7T SRAM using Sleep Transistor

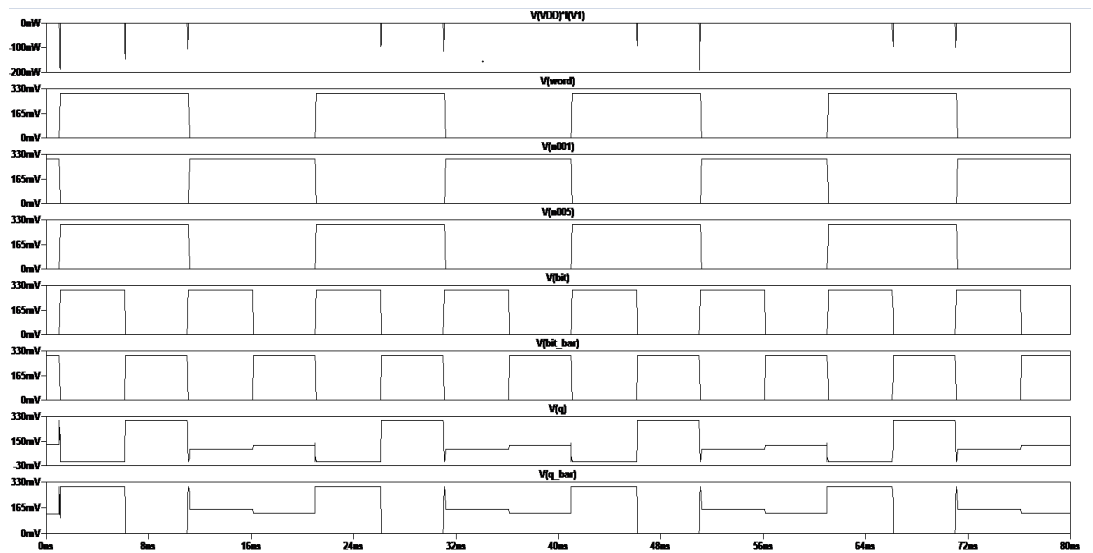


Fig.10 Waveforms of 7T SRAM using Sleep Transistor

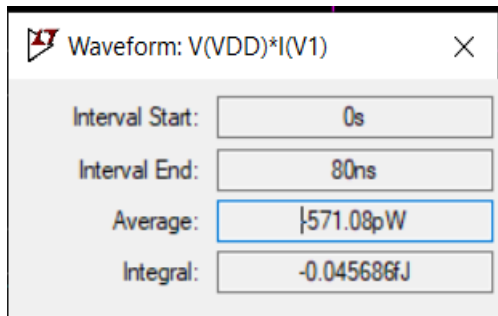


Fig. 11 Average Power

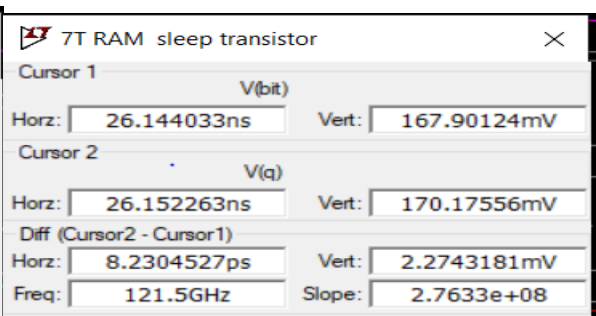


Fig.12 Delay

- Power Delay Product (PDP): The product of power dissipation and propagation delay, indicating overall efficiency.

$$PDP=P\times t_{pd}= 46.999\times10^{-22}W.Sec \text{ (Joule)}$$

- Energy Delay Product (EDP): The product of energy consumed and delay, providing a comprehensive measure of performance.

$$EDP=E\times t_{pd}= P\times t_{pd}^2= 3.868\times10^{-32}J.Sec$$

5.3 Power Dissipation and Delay of 7T SRAM using Dynamic threshold MOSFET (DTMOS)

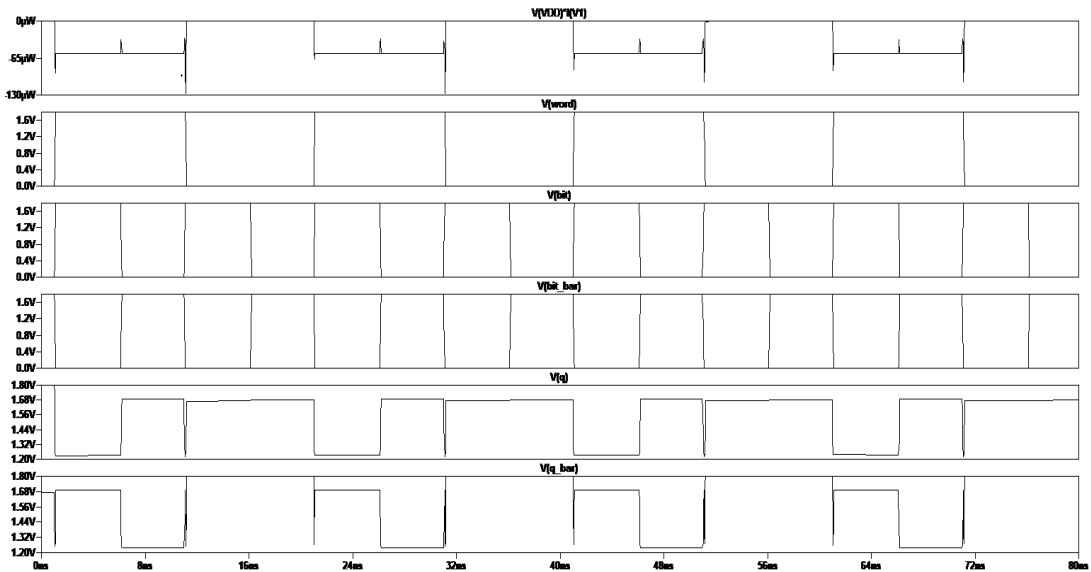


Fig.13 Waveforms of 7T SRAM using Dynamic threshold MOSFET (DTMOS).

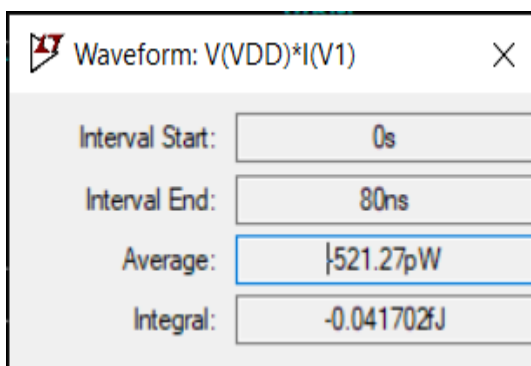


Fig. 13 Average Power

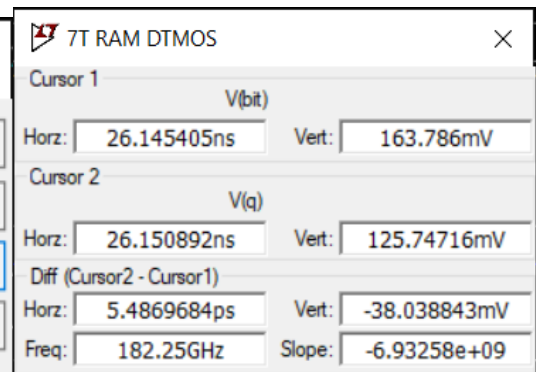


Fig.14 Delay

- Power Delay Product (PDP): The product of power dissipation and propagation delay, indicating overall efficiency.

$$PDP = P \times t_{pd} = 28.60 \times 10^{-22} \text{ W.Sec (Joule)}$$

5.4 Power Dissipation and Delay of 7T SRAM using Transistor Stacking

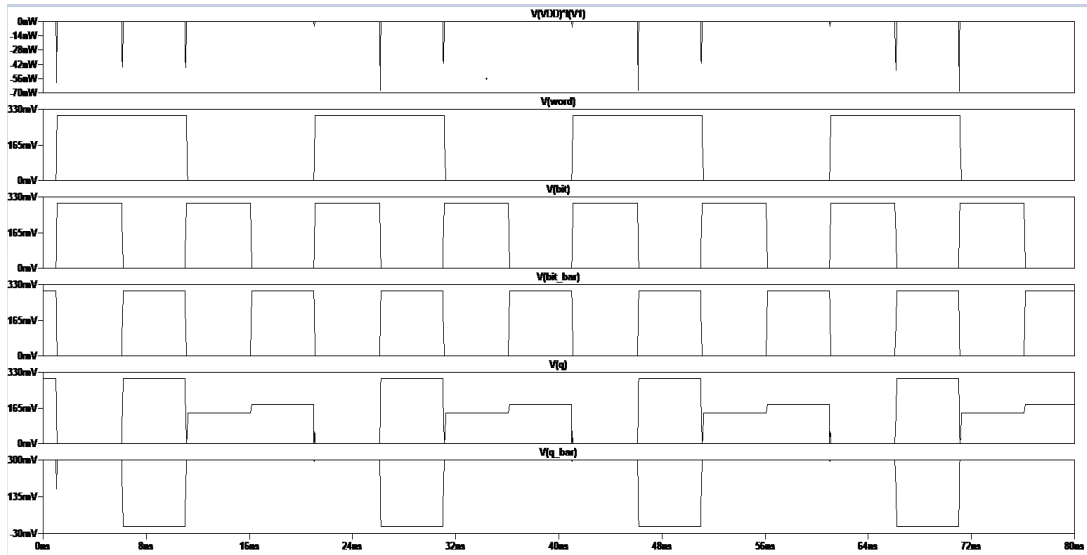


Fig.15 Waveforms of 7T SRAM using Transistor Stacking.

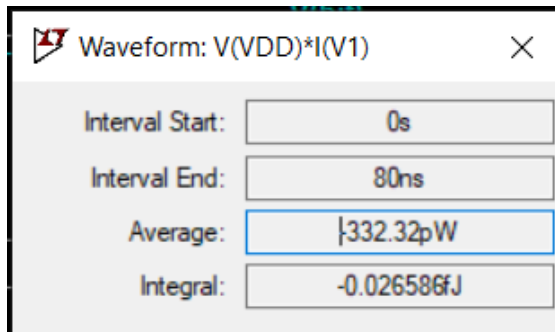


Fig. 16 Average Power

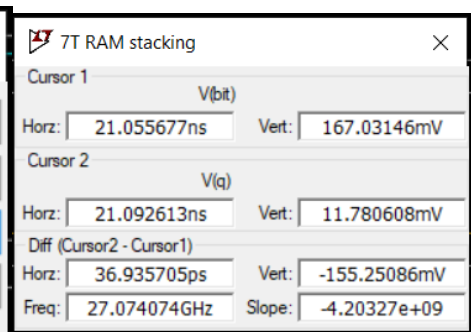


Fig.17 Delay

- Power Delay Product (PDP): The product of power dissipation and propagation delay, indicating overall efficiency.

$$PDP = P \times t_{pd} = 122.74 \times 10^{-22} \text{W.Sec (Joule)}$$

- Energy Delay Product (EDP): The product of energy consumed and delay, providing a comprehensive measure of performance.

$$EDP = E \times t_{pd} = P \times t_{pd}^2 = 45.33 \times 10^{-32} \text{J.Sec}$$

5.5 Power Dissipation and Delay of 7T SRAM using Dynamic threshold MOSFET (DTMOS) with Sleep Transistor

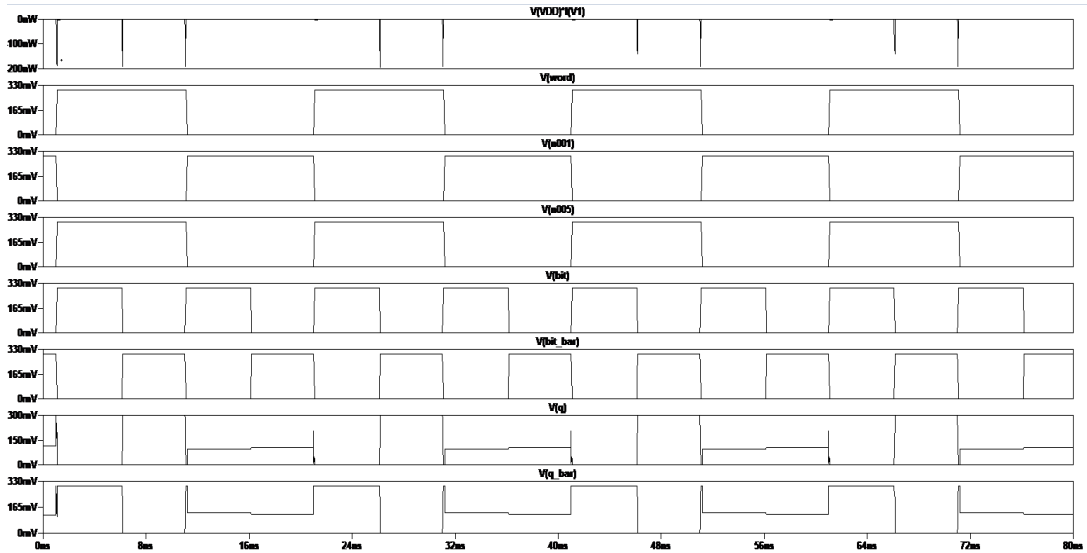


Fig.18 Waveforms of 7T SRAM using Dynamic threshold MOSFET (DTMOS) with Sleep Transistor.

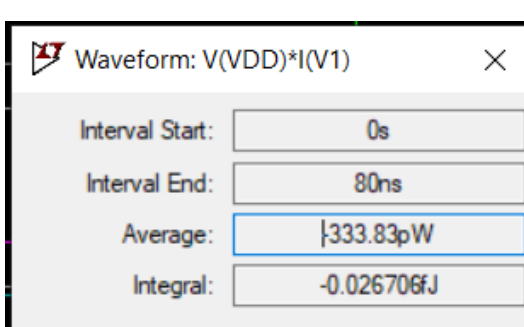


Fig. 19 Average Power

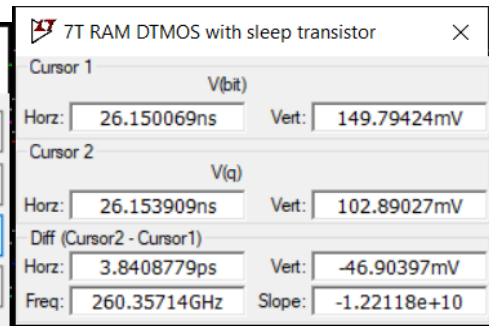


Fig.20 Delay

- Power Delay Product (PDP): The product of power dissipation and propagation delay, indicating overall efficiency.

$$PDP = P \times t_{pd} = 12.819 \times 10^{-22} \text{ W} \cdot \text{Sec (Joule)}$$

- Energy Delay Product (EDP): The product of energy consumed and delay, providing a comprehensive measure of performance.

$$EDP = E \times t_{pd} = P \times t_{pd}^2 = 0.492 \times 10^{-32} \text{ J} \cdot \text{Sec}$$

5.6 Power Dissipation and Delay of 7T SRAM using Stack Transistor with Sleep Transistor

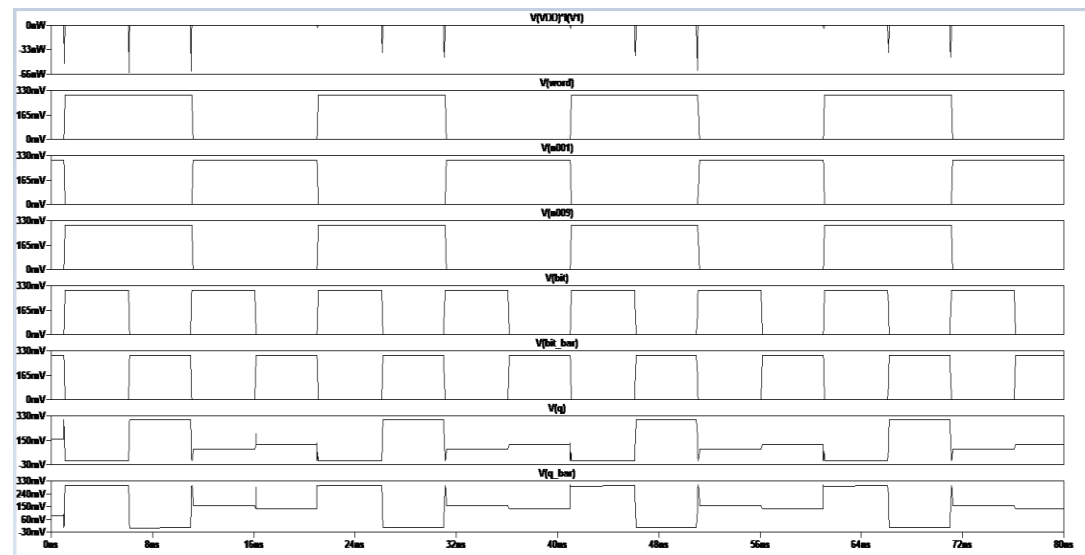


Fig.21 Waveforms of 7T SRAM using Stack Transistor with Sleep Transistor.

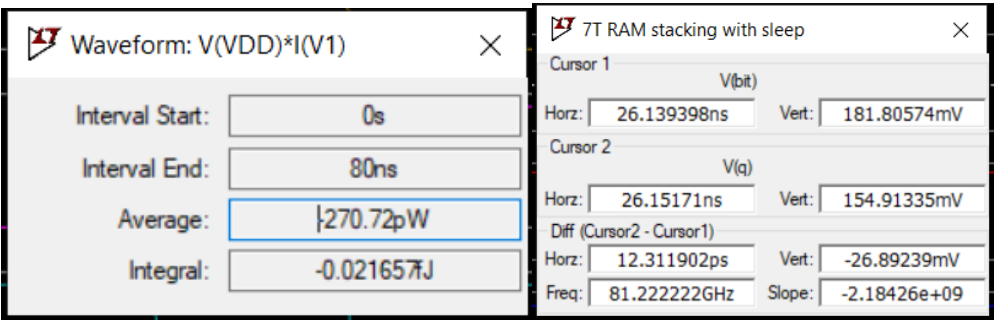


Fig. 22 Average Power

Fig.23 Delay

- Power Delay Product (PDP): The product of power dissipation and propagation delay, indicating overall efficiency.

$$PDP=P\times t_{pd}=23.9325\times10^{-22}W.Sec \text{ (Joule)}$$

- Energy Delay Product (EDP): The product of energy consumed and delay, providing a comprehensive measure of performance.

$$EDP=E\times t_{pd}=P\times t_{pd}^2=2.946\times10^{-32}J.Sec$$

6. Comparative Analysis

The comparative analysis highlighted that the DT MOS with Sleep technique offers the best balance between power dissipation and propagation delay. The Stack with Sleep technique provides the greatest power savings but at the cost of increased delay, making it suitable for

ultra-low-power applications where speed is less critical.

Technique	Power Dissipation (pW)	Propagation Delay (ps)	PDP(J) ($\times 10^{-22}$)	EDP(J.Sec) ($\times 10^{-32}$)
Basic 7T SRAM	914.38	32.92	301.023	99.099
Sleep Transistor	571.08	8.23	46.999	3.868
DTMOS	521.27	5.48	28.600	1.569
Transistor Stacking	332.32	36.93	122.74	45.330
DTMOS with Sleep	333.83	3.84	12.819	0.492
Stack with Sleep	270.72	12.31	23.932	2.946

7. Conclusion and Future Work

This paper demonstrated the effectiveness of various low-power techniques in the design of 7T SRAM cells. The combination of variable threshold and sleep transistors emerged as the most promising approach, offering significant power savings with minimal impact on performance. Future work could explore the scalability of these techniques to smaller technology nodes and their impact on other performance aspects like stability and noise margins. Additionally, incorporating adaptive control mechanisms could further enhance the efficiency of these designs.

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