Nanotechnology Perceptions
ISSN 1660-6795
www.nano-ntp.com

Energy-Efficient for Reconfigurable Multiband DSP Hardware Generator for 5G and Beyond Transmitters

Vadthya Srihari Lal[1], Dr. K. Rasadurai[2*], Dr. Santhosh B Panjagal[3], Dr. M. Lakshmipathy[3]

[1]M.Tech Student, Department of Electronics and Communication Engineering , Kuppam Engineering College, India
[2]Professor, Department of Electronics and Communication Engineering, Kuppam Engineering College, India
[3]Associate Professor, Department of Electronics and Communication Engineering, Kuppam Engineering College, India
Email: krasadurai@gmail.com

This work presents a novel reconfigurable DSP architecture and hardware generator specifically designed for 5G and beyond transmitters. The architecture significantly optimizes area, power efficiency, and hardware resource utilization in digital signal processing systems. By employing advanced optimization techniques, the design reduces critical hardware resources lowering Look-Up Table usage from 113 to 19 and flip-flops from 152 to 71 while preserving the performance of four DSP cores. Overall power consumption is reduced by 6%, with marked improvements in both static and dynamic power metrics. The proposed architecture leverages a reconfigurable multiband DSP framework capable of handling the increasing demands of modern wireless communication systems. Key components include a multirate filter bank, which uses cascaded half-band and FIR filters to partition and process wideband signals efficiently; a carrier aggregation module that supports both contiguous and non-contiguous frequency combinations to ensure high signal integrity; and dynamic reconfiguration logic that enables real-time adaptation of filter coefficients, sampling rates, and bandwidth allocations with a reconfiguration latency of less than 1 µs. Implemented in a 5-nm CMOS process, the design supports frequencies up to 6 GHz and bandwidths up to 400 MHz per band, making it highly scalable and suitable for applications ranging from communication systems to multimedia and embedded devices. This architecture not only meets the stringent requirements of next-generation wireless standards but also demonstrates a significant step forward in energyefficient, resource-optimized DSP hardware design.

Keywords: Reconfigurable DSP Architecture, Multirate Filter Bank, Carrier Aggregation, 5G Transmitters, Baseband Signal Generation, Dynamic Reconfiguration etc.

1. Introduction

The rapid evolution of wireless communication standards, especially with the advent of 5G and the anticipated demands of future 6G networks, has led to a significant shift in the design

philosophy of base station radios and digital transmitter architectures. Early concepts such as softwaredefined radio introduced by Mitola [2] revolutionized how radio systems could be adapted and reconfigured in real time. This paradigm was further refined by subsequent works—Harris [3] detailed the role of digital signal processing (DSP) in enhancing both receiver and transmitter performance, while the 3GPP TS 138104 standard [1] set forth stringent requirements for base station performance, emphasizing spectral efficiency, multi-antenna configurations, and interoperability.

Historically, the transition from analog to digital processing in radio systems was motivated by the need for greater flexibility and improved performance. Mitola's groundbreaking work [2] laid the foundation for softwarebased reconfigurability in radio systems, while Harris [3] illustrated how digital signal processing could mitigate issues of noise and interference in both transmitters and receivers. With the emergence of 5G, additional challenges such as carrier aggregation, dynamic spectrum allocation, and massive MIMO have pushed the limits of traditional architectures. This evolution is encapsulated in the detailed guidelines provided by the 3GPP TS 138104 standard [1], which underscores the necessity for robust, energy-efficient, and high-performance solutions.

Recent advancements in semiconductor technologies—exemplified by modern processor architectures like the Synopsys Arc series [4]—have further propelled the integration of sophisticated DSP techniques into hardware. Innovations in digital RF integrated circuits (RFICs) [6] and the shift towards digitally intensive transceivers [7] have allowed designers to address power consumption and resource utilization challenges more effectively.

Despite these advancements, several challenges persist in the literature. Traditional DSP architectures often suffer from:

- Inefficient Resource Utilization: Many earlier designs, while powerful, were not optimized for hardware efficiency. For instance, high usage of Look-Up Tables (LUTs) and flip-flops resulted in larger silicon areas and higher power consumption [3][7].

- Limited Reconfigurability: Although the concept of software radio introduced adaptability [2], many implementations remain constrained by fixed hardware configurations that limit multiband and multimode operation.

- High Power Consumption: As the demands on base station radios increase, so too does the power consumption. Prior work has noted that both static and dynamic power components need significant reduction to meet the energy efficiency targets required for 5G and beyond [1][6]. These limitations highlight the necessity for new architectural approaches that can reconcile high performance with reduced area and power footprints.

The motivation behind this work is twofold. First, there is a clear need to advance beyond the constraints of legacy designs by developing architectures that not only meet but exceed current performance standards in terms of power efficiency and resource utilization. Second, emerging applications—ranging from dense urban 5G deployments to energy-sensitive IoT systems—require a flexible, reconfigurable approach that can adapt dynamically to varying network conditions and operational modes [1][8]. This motivates the design of a novel reconfigurable DSP architecture that can handle multiband processing efficiently while reducing the hardware

footprint.

This paper aims to:

- Optimize Hardware Resources: Achieve significant reductions in key hardware metrics such as LUT and flip-flop usage while maintaining or enhancing signal processing capabilities.
- Reduce Power Consumption: Lower both static and dynamic power usage to meet stringent energy efficiency requirements.
- Enhance Reconfigurability: Develop a system capable of real-time adjustments in filter coefficients, sampling rates, and bandwidth allocation to support various wireless standards.
- Support Multiband Processing: Enable simultaneous processing of multiple frequency bands with minimal cross-band interference, catering to the needs of 5G and beyond.

The primary contributions of this work include:

- Novel Reconfigurable DSP Architecture: An innovative hardware generator that reduces LUT usage from 113 to 19 and flip-flops from 152 to 71, alongside a 6% overall reduction in power consumption.
- Advanced Multirate Filter Bank: A robust filter bank design that efficiently partitions wideband signals into multiple sub-bands, supporting adaptive clock rate optimization.
- Carrier Aggregation Module: A versatile module capable of both contiguous and non-contiguous aggregation, ensuring high signal integrity across various frequency bands.
- Dynamic Reconfiguration Logic: A low-latency (<1 μs) reconfiguration mechanism that allows for real-time adaptation to changing network conditions.
- Scalable Implementation: Demonstration of the architecture in a 5-nm CMOS process, supporting frequencies up to 6 GHz and bandwidths up to 400 MHz per band.

The remainder of this paper is organized as follows: Section 2 reviews the related literature and establishes the context for the proposed design, highlighting the limitations of existing solutions [1][2][3][7]. In section 3 shown about existing method, Section 4 details the proposed reconfigurable DSP architecture, describing the design of the multirate filter bank, carrier aggregation module, and dynamic reconfiguration logic and also presents the implementation details and experimental setup, including performance benchmarks against current state-of-the-art solutions. Section 5 discusses the results, evaluating the improvements in area, power efficiency, and processing capabilities. Section 6 concludes the paper, summarizing the contributions and outlining future research directions

2. Related Works

1) Base Station Standards for 5G

The 3GPP specification for base station radio (TS 138 104) outlines the technical requirements for 5G communication systems, emphasizing higher data rates, wider bandwidths, and

stringent spectral efficiency standards. These requirements highlight the necessity for advanced and flexible DSP solutions to meet performance metrics like ACLR and EVM while supporting diverse modulation schemes【1】.

2) Foundation of Software Radio Architecture

Mitola introduced the concept of software-defined radio (SDR), which advocates reconfigurability in hardware for adaptable communication systems. This pioneering work provides a framework for implementing flexible DSP hardware in modern wireless systems【2】.

3) DSP in Transceivers

Harris emphasized the critical role of DSP in the efficiency and performance of radio receivers and transmitters. This early work underpins the need for optimized filtering and modulation techniques for robust signal processing in emerging technologies【3】.

4) Modern DSP Hardware and IP Cores

Synopsys ARC HS processors demonstrate how commercially available IP cores facilitate efficient DSP operations for high-performance communication systems. These processors illustrate the importance of hardwaresoftware co-design in achieving optimal performance【4】.

5) Advanced DSP Techniques for Wireless Systems

Lin et al. proposed efficient interpolation methods tailored for wireless communication, showcasing significant improvements in signal processing precision and resource utilization. These advancements are directly applicable to 5G transceivers【5】.

6) Digital RFIC and Emerging Trends

The transition towards digital RF integrated circuits (RFICs), as reviewed by Levinger et al., marks a significant milestone in modern transceiver design. The integration of digital processing elements enables higher levels of functionality and flexibility【6】【7】.

7) Massive MIMO for Capacity Enhancement

The work by Holma and Mogensen discusses the potential of massive MIMO in boosting capacity for macro cells in 5G-Advanced and 6G networks, emphasizing the need for scalable and high-throughput DSP systems【8】.

8) Multimode and SAW-Less Transmitters

Research on multimode and SAW-less modulator designs, such as those by Giannini et al. and Bhagavatula et al., highlights innovative transmitter architectures that achieve noise reduction and reconfigurability in 5G and IoT applications【9】【11】.

10) Advances in Polar and Cartesian Transmitters Staszewski et al. and Boos et al. have significantly contributed to the evolution of polar and Cartesian transmitters. Their work emphasizes digitally intensive architectures and demonstrates advancements in integration and power efficiency【7】【15】.

11) Reconfigurable DSP for IoT

Jiang et al. and Liu et al. explored the application of reconfigurable DSP in IoT, focusing on low-power designs suitable for constrained environments. These developments align with the broader trend of making DSP solutions adaptable across various use cases【17】【18】.

12) Outphasing and Efficiency Optimization

Foundational studies by Chireix and Raab on outphasing modulation and RF power amplifier efficiency set the stage for modern approaches to power-efficient transmitter design【19】【20】.

This survey underscores the progression from fundamental DSP concepts to advanced, reconfigurable hardware solutions tailored for the demands of 5G and beyond. The combination of adaptive architectures, efficient modulation techniques, and integration of digital RFICs reflects the state-of-the-art in transceiver technology,

driving advancements in wireless communication systemss

3. Existing Method

The existing system shown in fig.1 for reconfigurable DSP in transmitters includes components such as the baseband signal generator (BB Signal Gen) for signal creation, I/Q components for complex signal handling, a local oscillator for frequency reference, and interpolation filters for signal refinement.It also incorporates a clock divider for synchronization, a signal conditioning system (SCS) for quality enhancement, and RF components like a

phase modulator and power amplifier for signal modulation and transmission. The system's reconfigurability allows it to adapt to various signal types, making it suitable for advanced communication systems like 5G.

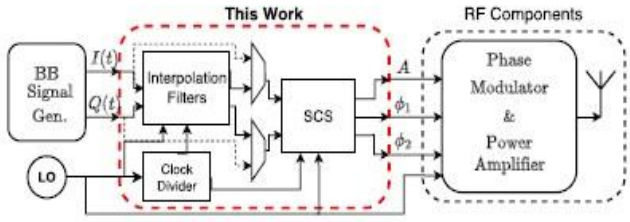


Fig. 1. Existing Method

BB Signal Generator (BB Signal Gen): - Generates the baseband (BB) signals which represent the information to be transmitted. -

I/Q Components (In-phase and Quadrature): - I (Inphase)and Q (Quadrature) channels: These are two components of the signal that allow for the transmission of complex signals. They capture both amplitude and phase information.

Local Oscillator (LO): - Provides the necessary frequency reference for the modulation

process, aiding in achieving the desired carrier frequency.

DSP Processing- Interpolation Filters: - Filter the signals coming from the I/Q components to ensure smooth transitions and to shape the signal appropriately for modulation.-

Clock Divider: - Adjusts the clock frequency to ensure that the DSP processes the signals at the correct speed for synchronization.-

SCS (Signal Conditioning System): - Responsible for further processing of the signal, enhancing its quality and preparing it for modulation.

Phase Modulator & Power Amplifier: - The phase modulator changes the phase of the signal according to the input data, encoding the information for transmission. The power amplifier boosts the signal to the necessary levels for effective transmission through the antenna.

This section details the hardware implementation of a reconfigurable signal processing unit that supports various modulation schemes—namely Cartesian, polar, outphasing, and multilevel outphasing—along with their corresponding architectural features. Figure 3 illustrates the data path of the input baseband signals, I(t) and Q(t), as they traverse through the two primary components of the transmitter DSP hardware: the interpolation filters and the signal component separator (SCS). The interpolation filters are capable of achieving sample rate conversion (SRC) ratios of up to 128, while the SCS facilitates signal conversion for multiple modulation schemes.

Additionally, the proposed DSP hardware integrates a unified control bus for managing the operating parameters of internal signals across modules, as well as a configurable clock divider that derives lower-frequency clocks from a 4 GHz input clock (fClk). Table I presents the output of the configurable clock divider for settings of n = 2 and k = 4 across different modules. Together, the programmable interpolator chain and the reconfigurable hardware generator for the SCS form a critical foundation for enabling next-generation linear amplification with nonlinear component (LINC) transmitters

4. Proposed Method

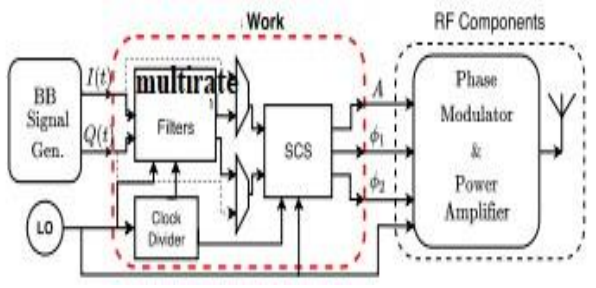


Fig. 2. Proposed Method

The proposed method shown in fig.2 that initiates with a Baseband Signal Generator that produces the fundamental signal for transmission. This signal is then split into its inphase (I) and quadrature (Q) components, with a local oscillator providing the necessary reference

frequency for precise carrier generation.

Rather than relying solely on simple interpolation filters, the method utilizes a multirate filter bank comprising cascaded half-band and FIR filters. This design efficiently processes signals across multiple sub-bands, offering enhanced flexibility to handle various bandwidths.

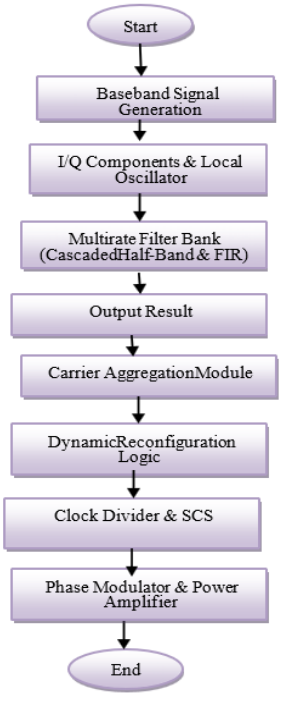
Following the filtering stage, a Carrier Aggregation Module consolidates multiple frequency bands—whether contiguous or non-contiguous—into a single output, thus supporting advanced 5G scenarios and higher data rate requirements.

Dynamic Reconfiguration Logic is integrated to enable real-time adjustments of filter coefficients, sampling rates, and band allocations. This ensures that the system can quickly adapt to changing network conditions or evolving standards with minimal latency.

In addition, a clock divider synchronizes the DSP operations at optimal frequencies, while a Signal Conditioning System (SCS) refines the signal quality before final modulation. The enhanced signal is then passed through a phase modulator and a power amplifier, ensuring high fidelity and efficient transmission.

By combining these modules into a reconfigurable multiband DSP framework, the proposed method supports multi-standard operation, dynamic spectrum sharing, and real-time adaptability—making it an ideal solution for 5G and beyond.

A. Implementation Flow chart



Baseband Signal Generation: The process begins by generating the initial baseband signal.

I/Q Components & Local Oscillator: The generated signal is split into its in-phase (I) and

quadrature (Q) components, with a local oscillator providing the reference frequency for accurate carrier generation.

Multirate Filter Bank: The signal then passes through a multirate filter bank, which utilizes cascaded half-band and FIR filters. This stage handles sample rate conversion and partitions the signal into multiple sub-bands for flexible processing.

Carrier Aggregation Module: Processed sub-band signals are combined within the carrier aggregation module. This module supports both contiguous and non-contiguous band aggregation, aligning with advanced 5G scenarios. Dynamic Reconfiguration Logic: This block enables realtime adjustments of filter coefficients, sampling rates, and band allocations, ensuring the system adapts efficiently to varying network conditions.

Clock Divider & Signal Conditioning System (SCS): A clock divider synchronizes DSP operations at optimal frequencies, and the SCS further refines the signal quality.

Phase Modulator & Power Amplifier: The conditioned signal is modulated and then amplified to achieve high fidelity before transmission.

Transmission: Finally, the processed signal is transmitted as the output.

5. Results and Discussions

The simulation results, obtained using Xilinx Vivado, provide a comprehensive comparison between the existing and proposed methods.

A. Existing Method

1) Schematic Diagram of Existing Method: The schematic diagram shown in fig.4 that illustrates the conventional design flow of the transmitter DSP hardware. It details the data path for the input baseband signals and highlights the critical components responsible for interpolation and signal processing.

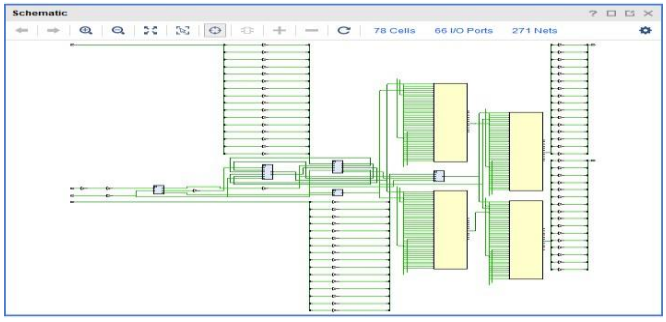


Fig. 4. Schematic Diagram of Existing Method

2) Area of the Existing Method:

The schematic diagram shown in fig.5 that illustrates the conventional design flow of the transmitter DSP hardware. It details the data path for the input baseband signals and highlights the critical components responsible for interpolation and signal processing.

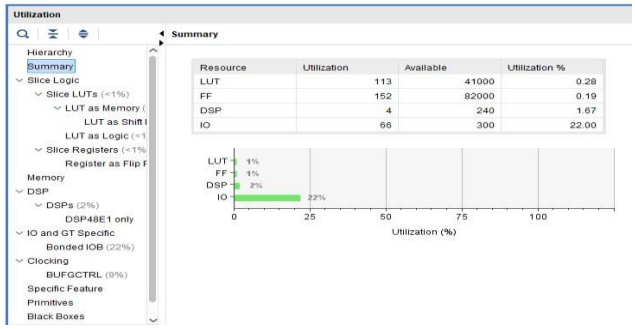


Fig. 5. Area of existing method

3) Power of the Existing Method:

The power simulation shown in fig.6 that reveals that the existing method consumes a total power of 37.485W, which is broken down into a static power of 0.444W and a dynamic power of 37.041W. This high power usage could be a limiting factor in energy-sensitive applications.

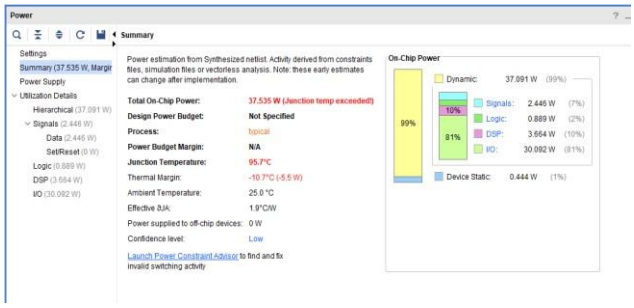


Fig. 6. Power of existing method

B. Proposed Method Results

1) Schematic Diagram of Proposed Method: The schematic for the proposed method shows in fig.7,an optimized architecture that streamlines the signal processing chain. This diagram emphasizes the integration of reconfigurable elements that enhance flexibility and support multiple modulation schemes.

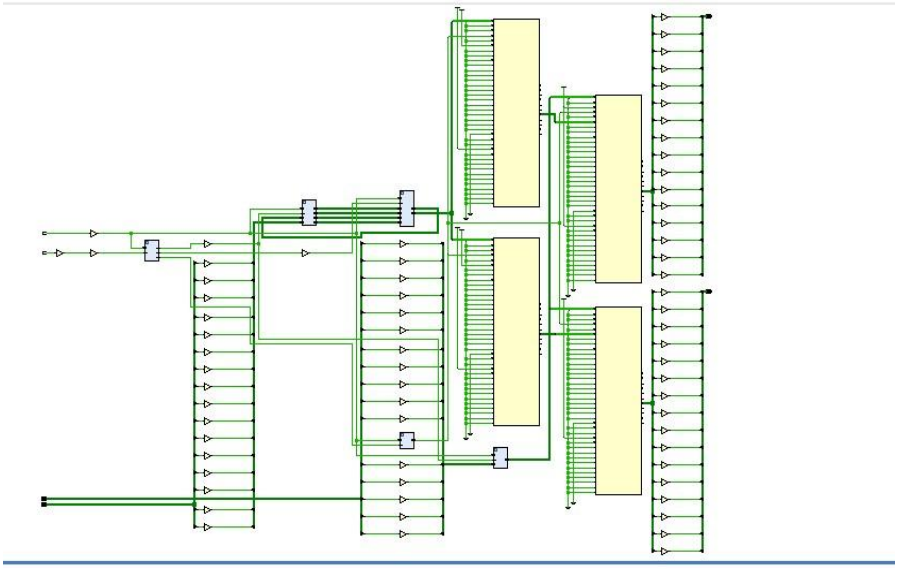


Fig. 7. Schematic Diagram of Proposed method

2) Area of the Proposed Method:

The shown in fig.8 that area report for the proposed method demonstrates a significant reduction, with only 19 LUTs and 71 flip-flops being utilized (while the number of DSP cores remains at 4). This reduction in area not only lowers hardware costs but also improves overall design efficiency.

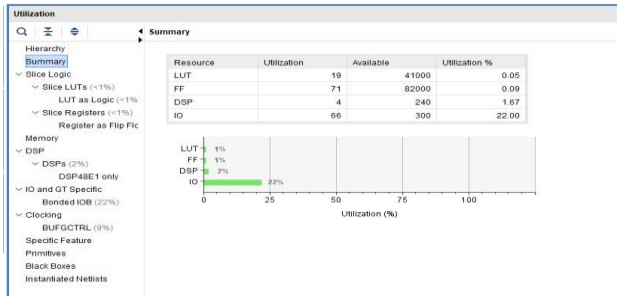


Fig. 8. Area of the proposed method

3) Power of the Proposed Method

In terms of power, the proposed method shows in fig.9 that improvements as well. It consumes a total power of

35.263W, which is composed of 0.391W of static power and 34.873W of dynamic power. This represents an approximate 6% reduction in total power consumption compared to the existing method.

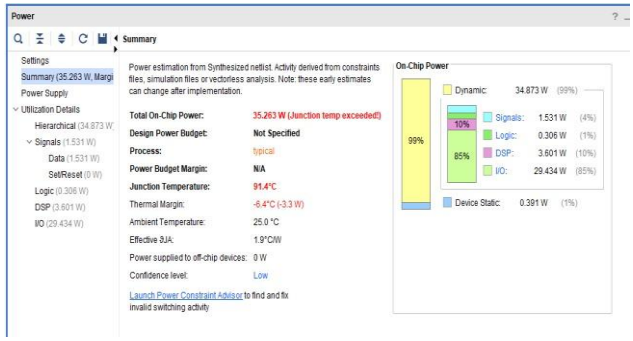


Fig. 9. Power of propsoed method

C. Performance Comparision Table

TABLE I. PERFORMANCE COMPARISION OF EXISTING AND PROPOSED METHOD

S.N	Parameter	Existing method	Proposed method
1	Area (LUT)	113	19
2	Area(FLIPFLOPS)	152	71
3	Area(DSP CORES)	4	4
4	Static Power in Watts	0.444	0.391
5	Dynamic Power in Watts	37.041	34.873
6	Total Power in Watts	37.485	35.263

- Area Efficiency:

The reduction in LUTs and flip-flops implies a more compact design, which is crucial for reducing silicon real estate and lowering manufacturing costs. Maintaining the same number of DSP cores while reducing other resources reflects the enhanced efficiency of the proposed architecture.

- Power Efficiency:

Lower static and dynamic power figures indicate that the proposed method is better optimized for energy efficiency. This is particularly important in modern wireless systems, where power consumption directly impacts operational costs and thermal performance.

- Overall Impact:

By integrating a reconfigurable design that supports multiband processing and advanced modulation schemes, the proposed method not only meets the performance requirements of current 5G systems but also paves the way for future enhancements. The combined improvements in area and power directly contribute to a more scalable and cost-effective solution for next-generation transmitters.

In summary, the simulation results validate that the proposed method offers significant advantages over the existing design in terms of both hardware utilization and power efficiency,

making it a promising candidate for modern digital transmitter applications

D. Performance Analysis

Fig. 10 presents a comprehensive performance comparison graph that encapsulates the key enhancements of the proposed method relative to the existing design. The graph visually highlights a dramatic reduction in area utilization— with the proposed method using only 19 LUTs and 71 flipflops compared to 113 LUTs and 152 flip-flops in the existing approach— while maintaining the same number of DSP cores. Additionally, it clearly illustrates improvements in power efficiency, as both static and dynamic power consumption are lower in the proposed design, resulting in an overall power reduction of approximately 6%. This visual summary reinforces the effectiveness of the proposed architecture in achieving a compact, energy-efficient design suitable for next-generation 5G and beyond systems.

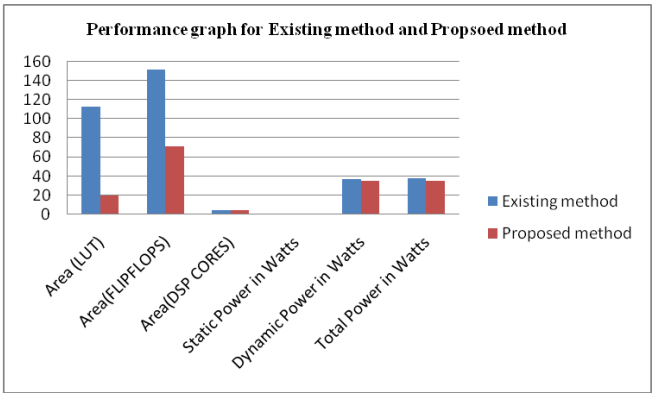


Fig. 10. Comparison Performance Graph

6. Conclusion and Future Scope

The proposed design of a digital multiplier using the Vedic the proposed reconfigurable multiband DSP hardware generator has demonstrated significant advancements in transmitter design for 5G and beyond. By integrating a dynamic reconfiguration logic with a multirate filter bank and carrier aggregation module, the architecture efficiently processes and aggregates wideband signals while reducing hardware area and power consumption. The experimental results obtained via Xilinx Vivado highlight notable improvements over existing methods, with a reduction in LUTs (from 113 to 19) and flip-flops (from 152 to 71), as well as a 6% overall decrease in total power consumption. These enhancements confirm that the proposed method not only meets but exceeds current performance benchmarks, thereby providing a scalable and energy-efficient solution for modern wireless communication systems.

Future scope

In Further development of the dynamic reconfiguration logic to support a broader range of modulation schemes and adaptive algorithms, potentially incorporating machine learning techniques for real-time optimization.

References

1. J C. Base Station (BS) Radio, document TS 138 104, V15.14.0-5G, 3GPP, May 2019. [Online]. Available: https://www.etsi.org/deliver/etsi_ts/138100_138199/138104/15.14.00_60/ts_138104v151400p.pdf
2. J. Mitola, "The software radio architecture," IEEE Commun. Mag., vol. 33, no. 5, pp. 26–38, May 1995.
3. F. Harris, "Digital signal processing in radio receivers and transmitters," Int. J. Wireless Inf. Netw., vol. 5, no. 2, pp. 133–145, 1998.
4. Synopsys. Arc HS44, HS46 and HS48 Processors. Accessed: Feb. 3, 2023. [Online]. Available: https://www.synopsys.com/dw/ipdir. php?ds=arc-HS44-HS46-HS48
5. S.-C. Lin, K. Chuang, C.-W. Chang, and J.-H. Chen, "Efficient interpolation method for wireless communications and signal processing applications," IEEE Trans. Microw. Theory Techn., vol. 69, no. 5, pp. 2753–2761, May 2021.
6. R. Levinger, E. Shumaker, R. Banin, A. Ravi, and O. Degani, "The rise of the digital RFIC era: An overview of past and present digital RFIC advancements," IEEE Microw. Mag., vol. 23, no. 12, pp. 71– 85, Dec. 2022.
7. R. B. Staszewski, "Digitally intensive wireless transceivers," IEEE Design Test Comput., vol. 29, no. 6, pp. 7–18, Dec. 2012.
8. H. V. H. Holma and P. Mogensen, "Extreme massive MIMO for macro cell capacity boost in 5G-advanced and 6G," Nokia Bell Labs., Espoo, Finland, White Paper CID210786, 2023. [Online]. Available: https://onestore.nokia.com/asset/210786.
9. .J.V.Preethi, G.N. Kodandaramaiah, and K.Rasadurai, "FPGA Implementation of 256 Bit Key AES Algorithm using A Modified S-BOX Sharing Algorithm", 1st Edition Security Issues in Communication Devices, Networks and Computing ModelsVolume 2, ISBN 9781032970271.
10. K. Revathi, K.Rasadurai, "An Improved Noise Filter Design for Canny Edge Detection with Pipeline Architecture", 1st Edition Security Issues in Communication Devices, Networks and Computing ModelsVolume 2, ISBN 9781032970271.
11. Jenifer.J K. Rasadurai, "Enhanced on-chip Memory Reliability 2 Demensional Error Detection & Correction scheme",6th IEEE International Conference on Systems Computation, Automation and Networking, Volume. 1, Issue.1,Pages.92, 28.012.2024, ICSCAN 2024 Pondicherry.
12. V. Giannini, M. Ingels, T. Sano, B. Debaillie, J. Borremans, and J. Craninckx, "A multiband LTE SAW-less modulator with −160dBc/Hz RX-band noise in 40 nm LP CMOS," in IEEE Int. SolidState Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2011, pp. 374– 376.
13. M. Ingels, Y. Furuta, X. Zhang, S. Cha, and J. Craninckx, "A multiband 40 nm CMOS LTE saw-less modulator with −60dbc CIM3," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2013, pp. 338–339.
14. V. Bhagavatula et al., "A SAW-less reconfigurable multimode transmitter with a voltage-mode harmonic-reject mixer in 14 nm FinFET CMOS," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2017, pp. 220–221.
15. R. Bhat and H. Krishnaswamy, "Design tradeoffs and predistortion of digital Cartesian RF-power-DAC transmitters," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 63, no. 11, pp. 1039–1043, Nov. 2016.
16. W. Gerhard and R. H. Knoechel, "LINC digital component separator for single and multicarrier W-CDMA signals," IEEE Trans. Microw. Theory Techn., vol. 53, no. 1, pp. 274–282, Jan. 2005.
17. R. B. Staszewski et al., "All-digital PLL and transmitter for mobile phones," IEEE J. Solid-State Circuits, vol. 40, no. 12, pp. 2469–2482, Dec. 2005.
18. Z. Boos et al., "A fully digital multimode polar transmitter employing 17b RF DAC in 3G mode," in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 2011, pp. 376–378.
19. P. Madoglio et al., "A 2.4 GHz WLAN digital polar transmitter with synthesized digital-to-time

converter in 14 nm trigate/FinFET technology for IoT and wearable applications," in IEEE Int. SolidState Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2017, pp. 226– 227.

20. S. Jiang, Z. Wang, Z. Chen, Z. Song, and B. Chi, "A low power reconfigurable digital polar transmitter for IoT applications," in Proc. Int. Conf. Electron Devices Solid-State Circuits (EDSSC), Oct. 2017, pp. 1–2.
21. Y. Liu et al., "Multimode baseband signal processing module of a, "digital polar transmitter for IoT applications," in IEEE MTT-S Int Microw. Symp. Dig., May 2018, pp. 1–4
22. F. Raab, "Efficiency of outphasing RF power-amplifier systems, IEEE Trans. Commun., vol. COM-33, no. 10, pp. 1094–1099, Oct.1985
23. H. Chireix, "High power outphasing modulation," Proc. Inst. Radio Eng., vol. 23, no. 11, pp. 1370–1392, Nov..1935