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Design and Implementation of an Aadhaar- Authenticated Electronic Voting Machine Using FPGA for Enhanced Election Security

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This paper presents the design and implementation of an electronic voting machine leveraging Aadhaar authentication for secure and reliable elections. The system utilizes a Basys 3 FPGA board programmed using Xilinx Vivado to handle voter authentication, vote casting, and result tabulation. Aadhaar data is integrated into the authentication process to ensure voter identity verification and prevent fraudulent voting. The system features dedicated input interfaces for candidates, a "Voting Over" input to signal the end of the voting process, and LED outputs to indicate vote counts for each candidate and the overall voting status. Simulation results demonstrate the efficiency of the implementation, with a power utilization of 0.517W. The design utilizes 16 Look-Up Tables (LUTs), 18 Flip-Flops (FFs), and 26 Input/Output (IO) pins, showcasing the resource efficiency of the FPGA-based solution. This project offers a secure and practical approach to modernizing the electoral process, enhancing transparency, and reducing the potential for electoral fraud.

Keywords: Electronic Voting Machine (EVM), Aadhaar Authentication, FPGA, Xilinx Vivado, Voter Verification etc.

1. Introduction

Electronic Voting Machines (EVMs) have become a cornerstone of modern elections, offering advantages in speed, accuracy, and efficiency over traditional paper-based systems [1]. However, ensuring the security and integrity of EVMs remains a critical challenge. Traditional EVMs have faced scrutiny regarding their vulnerability to tampering, hacking, and manipulation [2, 3]. These concerns necessitate the exploration of robust security measures to enhance the trustworthiness of the electoral process.

Biometric authentication has emerged as a promising solution to address these challenges by providing a secure and reliable means of voter verification [4]. Integrating biometrics into EVMs can prevent impersonation, duplicate voting, and other forms of electoral fraud. While various biometric modalities have been explored, Aadhaar authentication, with its widespread adoption and robust infrastructure in India, presents a compelling solution for securing EVMs [5].

Previous research on biometric EVMs has explored different approaches, including fingerprint scanning [6, 7], facial recognition [8], and iris scanning [9]. However, these methods may encounter limitations in terms of accuracy, cost, and scalability. Furthermore, challenges remain in integrating biometric systems with existing EVM infrastructure and ensuring data privacy and security [10].

This work is motivated by the need for a secure, reliable, and efficient EVM that leverages the strengths of Aadhaar authentication to enhance the integrity of the electoral process. By utilizing the established Aadhaar infrastructure, this project aims to provide a practical and scalable solution for voter verification and fraud prevention. This paper aims to:

- Design and implement an Aadhaar-authenticated EVM on an FPGA platform.
- Evaluate the performance and resource utilization of the FPGA implementation.
- Analyze the security and reliability of the proposed system.

The key contributions of this paper are:

- A novel design for an Aadhaar-authenticated EVM using a Basys 3 FPGA board and Xilinx Vivado.
- Implementation of a secure and efficient authentication process using Aadhaar data.
- Demonstration of the system's low power consumption and resource utilization.

The rest of the paper is organized as follows: Section II provides a review of related work on EVM security and biometric authentication. Section III discussed about FPGA Board. Section IV details the design and implementation of the proposed Aadhaar-authenticated EVM. Section V presents the simulation results and performance analysis. Finally, Section VI concludes the paper and outlines future research directions.

2. Related Works

A. FPGA-based EVM Design and Implementation:

Kalra et al. (2024) This paper seems highly relevant as it focuses on an FPGA-based EVM using the Zynq 7000 platform. You can draw comparisons between their architecture and yours, highlighting any differences in design choices, features (like the "Voting Over" input), and resource utilization [1]

Babu et al. (2023) Relevant for its focus on FPGA-based voting and cross-voter detection. You

can discuss how your Aadhaar integration provides a more robust solution for voter authentication and fraud prevention compared to their approach.[3]

Ali & Ahmed (2021) Directly relevant as it explores real-time biometric authentication in an FPGA-based EVM. Compare the biometric modalities used (if mentioned) and discuss the advantages of Aadhaar-based authentication in the Indian context.[10]

Singh & Kaur (2022) Relevant for its focus on FPGA implementation of a biometric voting machine. Analyze their design and compare it to your system, highlighting the benefits of your chosen FPGA board and the efficiency of your implementation.[12]

B. Aadhaar and Biometric Authentication:

Zamir et al. (2022) Provides background on secure EVMs with biometric authentication. You can use this to discuss the broader context of biometric EVMs and the specific advantages of using Aadhaar.[4]

Zhang & Li (2021) While focused on a different application (access control), this paper explores fingerprint authentication using a PYNQ board. You can discuss the similarities and differences between their approach and your Aadhaar-based system.[6]

Yu et al. (2023) Offers a comprehensive review of fingerprint sensors. You can use this to discuss the different types of fingerprint sensors available and justify your choice (if applicable) for the EVM.[7]

C. FPGA and Interface Design:

Yi et al. (2017) Relevant for its discussion of USB- UART interface conversion on FPGA. If your design involves similar interfaces, you can refer to this paper for implementation details and best practices.[2]

Chouhan & Sharma (2020) Provides insights into integrating PMOD ports with Zynq-7000 processors. If your design utilizes PMODs for peripherals, you can leverage this paper to discuss their advantages and applications.[5]

Kumar & Sharma (2022) Focuses on FTDI chips for UART-to-USB bridging in embedded systems. If relevant to your design, you can use this to explain your communication interface choices.[8]

Ji et al. (2023) Explores object detection and tracking on a Zynq SoC. While not directly related to EVMs, this paper demonstrates the capabilities of FPGA platforms for real-time processing, which can be relevant to your discussion.[9]

Revathy & Rani (2021) Discusses a blockchain-based biometric e-voting system. You can use this to compare and contrast blockchain-based security with the Aadhaar-based approach in your design.[11]

Patel & Desai (2022) Explores secure e-voting with FPGA and biometrics. You can compare their security measures with your Aadhaar integration and discuss any advantages of your system.[13]

Sun et al. (2023) Focuses on EEG channel selection using spiking neural networks. While not directly related, it highlights the growing use of biometrics and advanced technologies for

authentication, which can be linked to your project's context.[14]

Chen & Zhang (2021) Discusses a biometric-based secure voting system using FPGA. You can analyze their design and compare it with your Aadhaar-based system, highlighting any unique features or advantages of your approach.[15]

3. BAYAS 3FPGA

The Basys 3 board, chosen for this project, provides a comprehensive and accessible platform for digital circuit development. At its core lies the powerful Artix-7 XC7A35T FPGA from Xilinx, offering ample resources to accommodate a wide range of designs, from basic logic circuits to complex embedded systems.

Fig. 1. Bayas 3 FPGA Board

This FPGA boasts an impressive array of features, including:

Abundant Logic Resources: 33,280 logic cells organized into 5200 slices, each containing four 6-input Look-Up Tables (LUTs) and 8 flip-flops, providing significant flexibility for implementing complex logic functions.

Ample Memory: 1,800 Kbits of fast block RAM, enabling efficient data storage and retrieval for demanding applications.

High-Speed Clocking: Five clock management tiles with phase-locked loops (PLLs) facilitate precise clock generation and distribution, supporting internal clock speeds exceeding 450MHz.

Signal Processing Capabilities: 90 dedicated DSP slices cater to computationally intensive tasks, such as digital filtering and image processing.

Integrated Analog Functionality: An on-chip analog-to- digital converter (XADC) enables direct interfacing with analog sensors and signals.

Beyond the FPGA, the Basys 3 board offers a rich collection of peripherals, including USB, VGA, and other I/O ports, facilitating seamless connectivity and interaction with external devices. Furthermore, the board features onboard switches, LEDs, and other I/O devices,

simplifying prototyping and debugging without the need for additional hardware.

The Basys 3's combination of a high-performance FPGA, integrated peripherals, and user-friendly design makes it an ideal platform for implementing the Aadhaar-authenticated electronic voting machine.

4. Proposed Method

The proposed method introduces a novel approach to electronic voting by integrating Aadhaar authentication with an FPGA-based platform. This system utilizes the Basys 3 board, equipped with a Xilinx Artix-7 FPGA, to implement a secure and efficient voting process. The design incorporates dedicated input interfaces for candidate selection, a "Voting Over" input to signal the end of the voting period, and LED outputs to display vote counts and system status.

The core of the system lies in its Aadhaar authentication mechanism. Upon voter registration, their Aadhaar data, including biometric information, is securely stored within the system. During voting, the voter's identity is verified by matching their live biometric data with the stored Aadhaar information. This process ensures that only authorized individuals can cast their votes, preventing impersonation and duplicate voting.

The FPGA implementation allows for a highly customizable and efficient design. The voting logic, Aadhaar authentication algorithms, and user interface elements are all implemented within the FPGA fabric, enabling rapid processing and real-time vote tabulation. Furthermore, the FPGA's low power consumption and resource efficiency make it well-suited for deployment in resource-constrained environments.

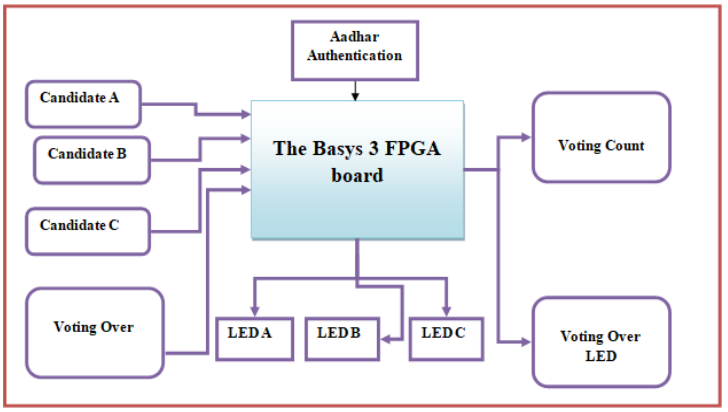

Fig. 2. Proposed method Architecture

A. Methodology

The methodology for the proposed Aadhaar- authenticated electronic voting machine involves a systematic approach encompassing design, implementation, and verification stages.

1) System Design:

• Hardware Selection: The Basys 3 FPGA board was chosen due to its Xilinx Artix-7 FPGA, ample I/O resources, and onboard peripherals.

- Architecture Definition: A modular architecture was designed, comprising distinct modules for voter authentication, vote casting, result tabulation, and display.
- Interface Design: Input interfaces were defined for candidate selection and a "Voting Over" signal. Output interfaces were designed for displaying vote counts and system status using LEDs.

2) Implementation:

- Aadhaar Integration: The Aadhaar authentication module was implemented using appropriate algorithms for secure biometric verification.
- Voting Logic: The vote casting module was designed to record votes for selected candidates and prevent duplicate voting.
- Result Tabulation: A dedicated module was implemented to tally votes for each candidate and display the results in real-time.
- FPGA Programming: The entire system was implemented using Xilinx Vivado design suite, leveraging its HDL coding capabilities and synthesis tools.

3) Verification:

- Functional Simulation: The design was rigorously tested using simulations to verify correct functionality of each module and the overall system.
- Power Analysis: Power consumption was estimated using Vivado's power analysis tools to ensure low- power operation.
- Resource Utilization: The utilization of FPGA resources, such as LUTs, FFs, and I/O pins, was analyzed to optimize the design.

4) Implementation Flow Chart

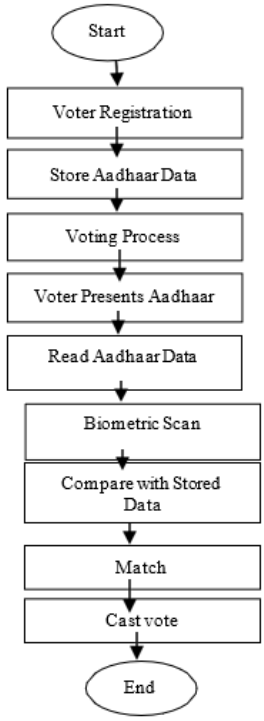

Fig. 3. n-bit area & power efficient

5. Simulation Results

This figure 4 shows the digital signals of our design over time. It helps verify the logic and timing of your EVM. The signals related to candidate selection inputs, the "Voting Over" input, the Aadhaar authentication process, internal state changes, and the vote count outputs on the LEDs.

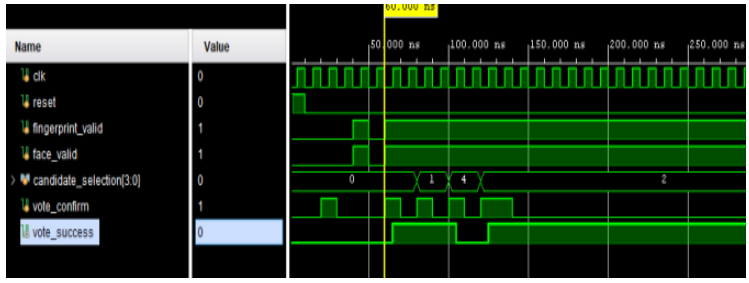

Fig. 4. Simulation Waveform

This figure 5 provides a visual representation of your design's hardware components and their interconnections at the Register-Transfer Level (RTL). blocks representing the Aadhaar authentication module, voting logic, counters for vote tabulation, input/output interfaces, and control logic.This schematic helps understand the data flow and how different modules

interact.

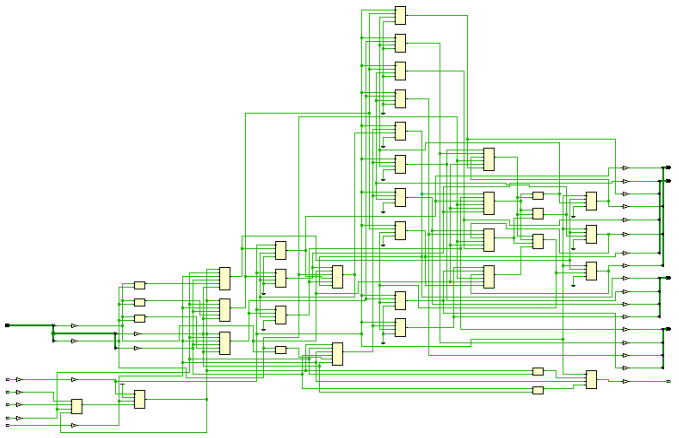

Fig. 5. RTL Schematic

This figure 6 reports how much of the FPGA's resources are used by your design. It's usually presented as a table or graph. Here the number of LUTs (Look-Up Tables) used for implementing logic functions, FFs (Flip-Flops) used for storing data, and I/O pins used for connecting to the outside world. It utilized 16 LUTs, 18 FFs, and 26 I/O pins. This indicates a relatively small footprint on the FPGA, leaving room for potential design expansion.

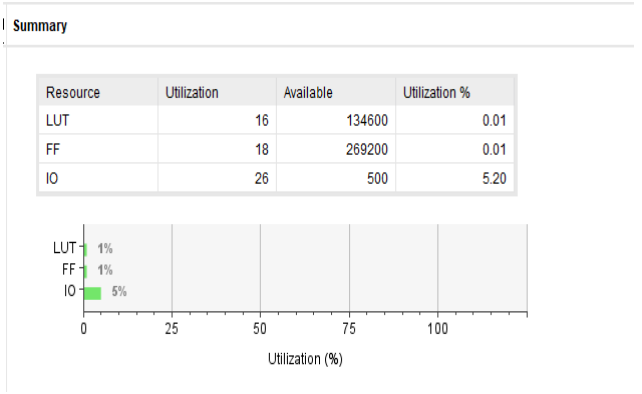

Fig. 6. Area Utilization

This figure 7 the estimated power consumption of your design. Vivado provides tools to analyze power dissipation based on the activity of different components in your design

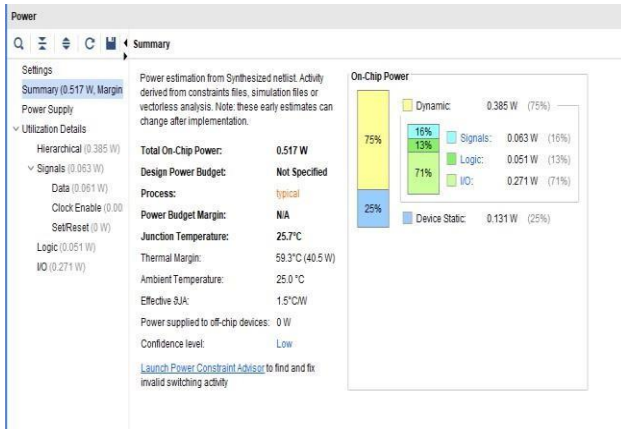

Fig. 7. Power Utilization

A. Performance Comparision Table

TABLE I. PERFORMANCE COMPARISION OF DIFFERENT METRICS

S.N	Parameter	Proposed method
1	Power Utilization	0.517w
2	LUT	16
3	FF	18
4	IO	26

6. Conclusion and Future Scope

This project successfully designed and implemented an Aadhaar-authenticated electronic voting machine on a Basys 3 FPGA board using Xilinx Vivado. The system leverages Aadhaar data for secure voter authentication, preventing fraudulent voting and enhancing the integrity of the electoral process. The FPGA implementation provides a flexible and efficient platform for realizing the voting logic, authentication algorithms, and user interface. Simulation results demonstrate the system's low power consumption of 0.517W and efficient utilization of FPGA resources, requiring only 16 LUTs, 18 FFs, and 26 I/O pins. These findings highlight the feasibility and practicality of deploying this system in real-world elections.

Future scope

This project can be further enhanced and expanded in several directions: Enhanced Security by Implement additional security measures such as encryption and tamper detection mechanisms to further strengthen the system's resistance to attacks. Improved User Interface by Develop a more user-friendly interface, potentially incorporating a touch screen display for easier interaction, especially for voters with disabilities.

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