Nanotechnology Perceptions
ISSN 1660-6795
www.nano-*ntp.com*

Investigation On Next-Generation Low-Power Design Methodologies For VLSI Circuits

Rekha Yadav[1] , Rajni[2]

[1,2]*ECED Deenbandhu Chhotu Ram University of Science and technology, Murthal*
rekhayadav.ece@dcrustm.org

The high rate of growth of portable electronics, Internet of Things (IoT) devices, and high-performance computing systems has further accelerated the need of efficient energy design of Very Large Scale Integration (VLSI) designs. Power consumption has become a design concern giving the battery life, device reliability and system performance a direct impact. This paper outlines an extensive literature review on next generation low-power design-methodologies that tackle dynamic, static, and leakage power issue in modern circuits. Different methods, including multi-threshold CMOS, power gating, clock gating, dynamic voltage and frequency scaling (DVFS) and near-threshold computing are discussed. New strategies at device and architecture levels are also presented, where the area overhead, power efficiency, and performance trade-offs are also considered. In addition, the paper identifies the recent developments in machine-learning-based power optimization and the issue of ultra-low-power designs that can be made possible with the help of advanced fabrication technologies. The discussion ends by providing thoughts on the future of the research and indicates how new low-power methods can facilitate sustainable and scalable VLSI systems in future applications.

Keyword: VLSI circuit, Low Power, CMOS, Machine Learning.

1. Introduction

The accelerated rate of the digital technology has already brought an unparalleled necessity in using electronic systems with a remarkable number of functionalities and high performance. Very-Large-Scale Integration (VLSI), which is essentially a key element in the modern electronics that makes it possible to place millions (and even billions) of transistors on a single chip, is at the heart of this evolution. The most important design constraint of VLSI circuits is now power consumption, including such aspects as thermal management of high-performance computing systems and battery life of mobile devices[1].

Traditionally, power consumption in VLSI designs has been relegated to the second place to other factors like speed and area efficiency. Energy efficiency has recently become the buzzword with the opening of energy efficient data centers, mobile computing, and the Internet of Things (IoT), where energy efficiency needs to be taken into account at all levels of design, including system architecture as well as at transistor implementation level. This change has

driven the emergence of next-generation low-power design methods towards providing a fine balance between dependability, power and performance.

These techniques cover a wide range of practices as multi-threshold CMOS (MTCMOS), clock gating, power gating, dynamic voltage and frequency scaling (DVFS), and near-threshold computing among others. The strategies focus on different dissipation points of power, including leakage, statical and dynamic, and provide novel methods of reducing them. Also, incorporating artificial intelligence and machine learning into electronic design automation (EDA) tools also allows predictive and adaptive power management, further improving the efficiency of VLSI systems.

Low-power design becomes more difficult due to the limitations of the traditional CMOS scaling - which are becoming apparent, as devices scale near the physical limits of the Moore Law. This has led to the exploration of alternative technologies including carbon-nanotube transistors, tunnel field-effect transistors (TFETs) and FinFETs as potential future directions towards achieving power reduction without changing the computational integrity. Further, system-level solutions, such as approximate computing, energy-conscious scheduling, and hardware-software co-design, are also beginning to be seen as holistic solutions to the power crisis[2].

This paper examines the field of next-generation low-power design techniques of VLSI circuits with an in-depth discussion of all trends, new approaches, and future trends. The mission is through the analysis of the theoretical models as well as practical application to shed light on strategies that are transforming the post-scaling era of computing energy efficiency. The information presented herein is supposed to help technologists, engineers, and researchers in the development of VLSI systems that are high-performance and sustainable and thus to satisfy the dynamic demands of the current electronics.

2. Literature Review

The growing need of energy efficient systems in many fields, including high-performance computing and other fields like handheld electronics, has influenced the development of low-power design in VLSI circuits. Initial research was mainly aimed at the minimization of dynamic power, which was produced by digital circuit switching. Isolation of operands, restructuring logic and clock gating were also used in large numbers to reduce unnecessary transitions and save energy.

With the reduction of technology nodes, the contribution of the statical power especially leakage currents came to play as a large contributor to the total power consumption. The change led to the invention of techniques like multi-threshold CMOS (MTCMOS), power gating, and body biasing, which tried to reduce the leakage without affecting performance. These methods formed the basis of the more advanced power-management approaches in modern VLSI designs[1-2].

Dynamic Voltage and Frequency Scaling (DVFS) was a powerful concept of runtime power optimisation. DVFS ensures efficient operation of systems in different conditions due

to changes in voltage and frequency in response to workload requirements. Nevertheless, its effectiveness is constrained by latency, granularity and the overhead of voltage regulators. To overcome these limitations, scientists have considered near threshold computing (NTC), which runs circuits at voltages near to the transistor threshold. NTC is capable of massive power savings, but has issues of speed, variability, and reliability.

The recent years have seen the integration of machine learning with electronic design automation (EDA) to open new prospects of intelligent power management. Reinforcement learning algorithms, neural networks, and decision trees are starting to be used to inform the synthesis, placement and routing choices of power-sensitive selections. These data-driven approaches are able to change in line with design constraints and environmental conditions, and offer dynamic and context-sensitive optimisation.

In addition to standard CMOS technologies, research is also being done on new devices like FinFETs, tunnel field-effect transistors (TFETs), and carbon-nanotube field-effect transistors (CNTFETs) that have the potential of lowering power consumption. Sub-10nm nodes have adopted FinFETs, which are better electrostatically controlled. TFETs show ultra-low leakage and steep sub -thresholds, but their implementation is still a challenge. The CNTFETs have high mobility and high scalability and hence they are attractive candidates of future low-power systems. In spite of such developments, a number of weaknesses exist in the literature. A lot of them are very contingent on particular process technologies and are not easily generalised across platforms.

Further, design decisions remain challenging due to trade-offs between power, performance, area, and reliability. There is a requirement of cohesive frameworks incorporating optimisations at hardware level with system-level plans such as software-conscious power management and cross-layer co-design. The paper review provides insight into the diverse and dynamic low-power VLSI design environment. There has however been a considerable advancement; however, the body is still in need of novel, scalable, and adaptive approaches that would address the energy limitations of next-generation electronic systems[3-4].

3. Next-Generation Low-Power Design Methodologies

The approach that we have followed herein is a multi-layered approach which is aimed at tackling the growing problems of power consumption that are inherent to the modern VLSI systems in a systematic way. As more and more portable electronics, IoT, and high-performance computing platforms are created, energy efficiency has become a design challenge. This design approach combines both circuit-level, architectural-level, and system-level solutions to attain an optimal powerperformance ratio and be scalable and manufacturable.

A. Power Dissipation Analysis and Classification.

The methodology is based on the analysis of power dissipation processes in CMOS circuits where the detailed analysis is made. Power consumption is categorically divided into three types:

a) **Dynamic Power:** It is due to the charging and discharging of load capacitances during switching occurrences, and it increases with the square of the supply voltage and the switching frequency.
b) **Statical Power:** To a great extent this is due to leakage currents that remain when transistors are in the off state; it is more pronounced in deep submicron technology.
c) **Short Circuit Power**: Occurs during logic transitions when PMOS and NMOS devices are simultaneously conducting over a brief period of time[3-5].

B. Techniques of Circuit-Level Optimization.

In the transistor and gate level, a number of established methods are used to lower power consumption:

a) **Multi-Threshold CMOS (MTCMOS):** Multi-Threshold CMOS (MTCMOS) uses transistors with different threshold voltages. A non-critical path is where high-threshold devices are placed, which stops leakage, and a timing-critical path is one where low-threshold devices are used to maintain performance. The coexistence of high-threshold and low-threshold transistors and sleep transistorters in the standby mode, as illustrated in Figure 1(a), has the effect of minimizing leakage power[6-8].
b) **Power Gating:** Power gating is a powerful low-power VLSI design technique, which is useful to reduce leakage during idle states. It functions by applying sleep transistors to cutoff the power supply to blocks of inactive circuit thereby eliminating unnecessary dissipation of power. Logic states are stored on retention registers and invalid signals are gated out when the block is not active as seen in Figure 1(b). Stored states are restored once again on reactivation and regular operation is restored with significant energy savings without performance loss[9-11].

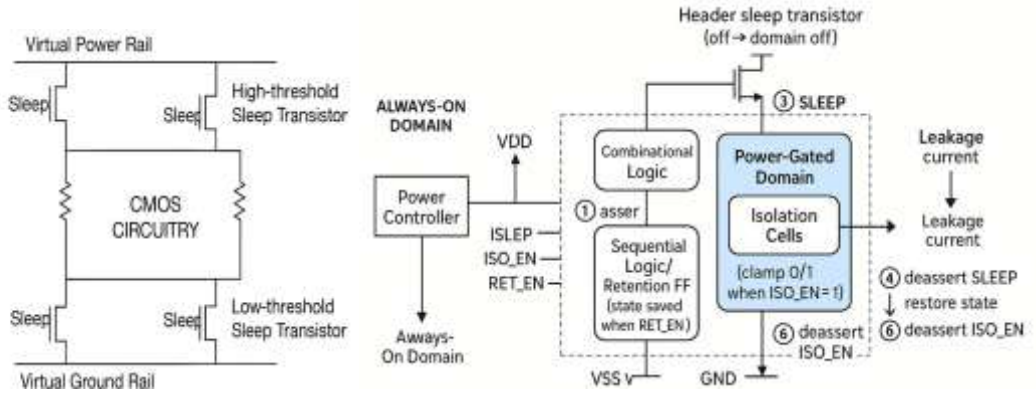
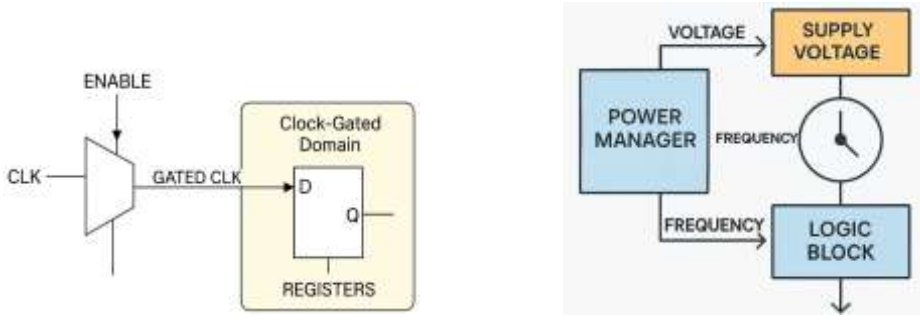


Figure 1: (a) Multi-Threshold CMOS methodology, and (b) Power-Grated low power Methodology

c) **Clock Gating:** Clock gating is a common low-power VLSI method used in the reduction of dynamic power. In place of the clock being propagated to all registers

and logic blocks, an enable signal determines the propagation of the clock. At enable low the clock is blocked so that unnecessary switching activity in the idle sections of the circuit is avoided as shown in Figure 2(a). Such selective clocking distribution reduces power usage and maintains proper operation of active modules[9-10].

d) Dynamic Voltage and Frequency Scaling (DVFS): Dynamic Voltage and Frequency Scaling (DVFS) is a dynamic voltage and frequency modulation technique used in conjunction with clock gating to accomplish dynamic power reduction. Instead of constantly driving the clock to all registers and logic blocks, an enable signal that governs the propagation of the clock is used. The enable is low in this case, which suppresses the clock, thus, avoiding any unwanted switching activity in the idle parts of the circuit as illustrated in Figure 2(b). This selective clock distribution manages to reduce the level of power consumption and maintain the correct functioning of active modules [12].



(a) (b)

Figure 2: (a) clock gating, and (b) DVFS Techniques to reduce power of VLSI circuits

e) Near-Threshold Computing: Near-Threshold computing Near-Threshold computing (NTC) is a power-efficient architecture in VLSI systems that can execute digital circuits at supply voltages close to the transistor threshold voltage. NTC reduces both dynamic and static power consumption by a significant margin by reducing the operating voltage, which makes it especially suitable to energy-compromised applications like wearables and sensor networks. In spite of the fact that performance may decrease over time because of slower switching speeds, NTC counteracts the disadvantage with parallelism and architecture optimization that preserve throughput shown in 3(a,b). This method is therefore particularly beneficial in very low power in which energy efficiency takes precedence over raw performance[13].

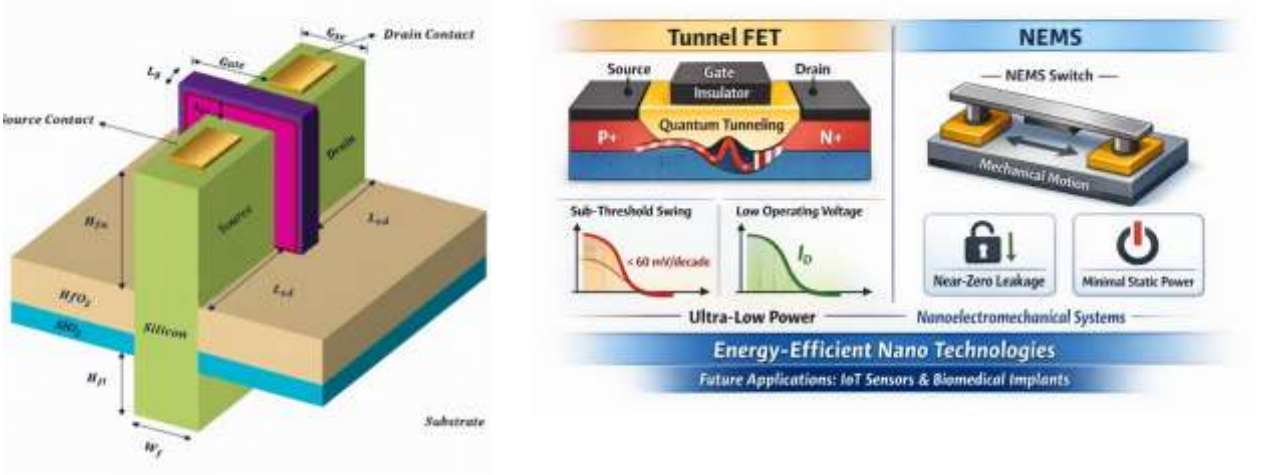
(a) (b)

Figure 3: (a) Near Threshold Computing, and (b) comparison of traditional and near threshold computing methodology

C. Device-Level Innovations

The methodology to supplement circuit-level techniques is to incorporate nascent device technologies providing inherent benefits in power:

a) **FinFETs and Gate-All-Around (GAA):** Transistors FinFETs and GAA transistors FinFETs and GAA Transistors are more efficient device architectures that have been shown to significantly improve power efficiency in VLSI design. FinFETs use a three-dimensional architecture, where the gate is covering a thin silicon fin, which provides



(a) (b)

Figure 4: (a) FinFET Structure, and (b) TFET & NEMS structure for low power VLSI circuits

higher control of the channels and the channeling of leakage currents [14,15]. GAA transistors extend this idea by completely enclosing the channel by a gate, which allows further narrowing of the electrostatic control and reduction of the threshold voltages. These designs reduce short-channel effects and allow aggressive scaling, making them the favorites of low-power performance-oriented uses in modern integrated circuits. The FinFET figure 4(a) below shows transistor architecture of three dimension, unlike the traditional planar architecture. It has a vertical silicon fin as its central feature which functions as the channel and the gate electrode is enclosed on all three sides. This type of multi-gate design gives better electrostatic control of the channel, greatly decreasing unwanted leakage currents and counteracting short-channel effects. The source, drain, high -k HfO 2 gate dielectric, and SiO 2 buried oxide are well defined. The new 3D architecture is essential in attaining high performance, reduced power usage and continued miniaturization of high end VLSI technology.

b) Nanoelectromechanical Systems (NEMS): Tunnel Field Effect Transistors (Tunnel FETs) and Nanoelectromechanical Systems (NEMS) are the current state of the art in the design of ultra-low power VLSI as in figure 4(b). Tunnel FETs are based on quantum tunneling instead of thermionic emission, allowing sub-threshold swings better than 60 mV/dec -1 of conventional MOSFETs. The property allows working with lower voltages and reduced power usage. NEMS devices also use nanoscale mechanical motion to perform switching functions with virtually zero leakage and low-static power. Combined, these technologies are pushing the limits of energy efficiency, and will be a promising platform in low-power electronics in the future, such as biomedical implants and IoT sensors. The innovations at the device level are considered in terms of their manufacturability, reliability and their ability to be integrated into the standard CMOS processes [16].

D. Architecture-Level Strategies

In addition to single-gate and transistor, choices made in architecture are crucial to optimizing power as shown in figure 5:

a) **Hierarchical Power Domains**: Hierarchical power domains subdivide the chip into various distinct domains, therefore, allowing functional blocks to be selectively activated and minimizing total power consumption.

b) **Resource Sharing and Reconfigurable Architectures**: This allows resources to be dynamically allocated according to workload and enhances resource utilization and minimizes idle power.

c) **Memory and Interconnect Optimization**: There are memory banking, data compression, and low-power interconnect protocol techniques used to cut the energy used in data movement and storage [17,18].

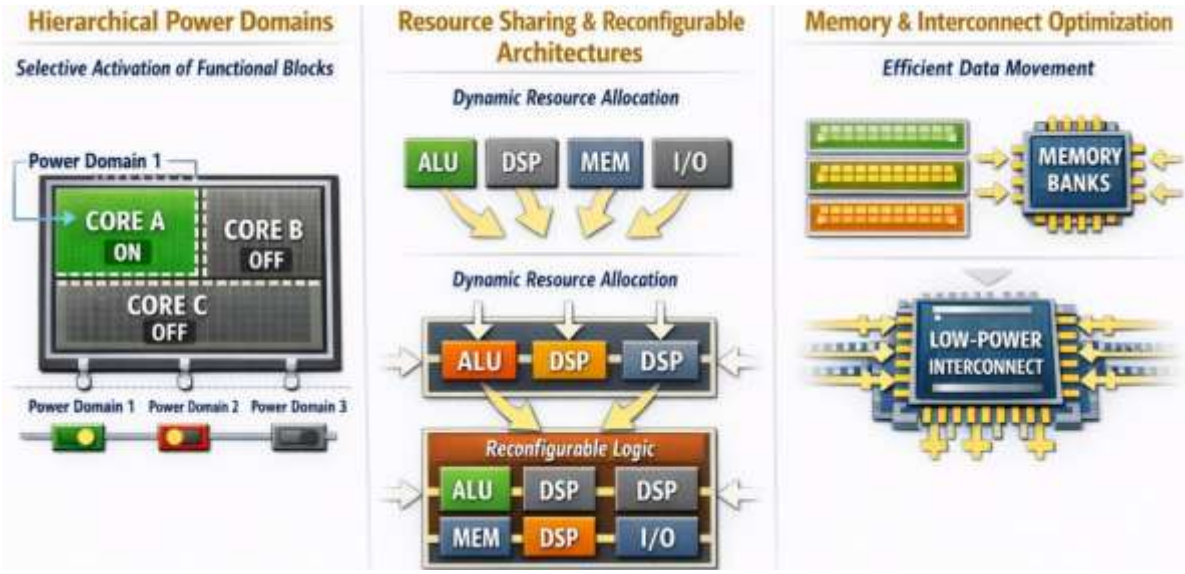


Figure 5: Comparison of three main architecheral level power optimization methodologies.

The aim of these strategies is to scale to various application areas, both embedded systems and high-performance processors.

E. Design Automation based on Machine Learning.

Since the modern VLSI design can be quite complex, the methodology incorporates the use of machine learning to automatically generate designs with optimized power consumption [19]:

a) **Predictive Modeling**: Predictive modeling of machine learning-based design automation is an innovative method of obtaining low power VLSI designs. Machine learning algorithms can predict patterns of power consumption using large amounts of data collected in the past, and the algorithm can determine the best design settings early during the design phase. This allows automated choice of voltage scaling, component choice and architecture trade-offs and saves a great deal of effort and design-space exploration. This means that predictive modeling assists engineers to design energy efficient circuits, with better performance, and reliability and therefore it is an important tool in the contemporary low power VLSI design process as shown in figure 6.

b) **Reinforcement Learning**: This is employed to search the design space and determine the best designs with regards to voltage scaling, clock gating, and placement.

c) **Clustering and Feature Selection**: The method assists in determining the important areas in the design that consume most power and can be optimized. This is a smart method of reducing design time and enhancing precision in power estimation and regulation.

Figure 6: Design automation based mashine learning techniques for low power.

F. Process-Aware Design and Fabrication

In order to make the methodology viable in practice, the following considerations in reference to fabrication technologies are taken into consideration:

- **Process Variation Modeling:** Due to process flaws in the production, variation in transistor features is modeled and provides reliable low-power operation.
- **Thermal Management**: Designs will be analyzed based on thermal hotspots and cooling needs, since too much heat may destroy performance and reliability.
- **Compatibility with Advanced Nodes**: Techniques are proven to be applicable to sub-10nm technology and 3D integration, with future proof designs.

Such considerations make sure that the suggested methodologies are not merely sound in theory but also can be produced and be used in the real world[20].

G. Trade-Off Analysis and Optimization Framework

Lastly, a multi-objective optimization model has been used to trade power, performance and area:

- **Energy-Delay Product (EDP):** This is a major measure that is employed to determine the efficiency of low-power techniques.
- **Power-Performance-Area (PPA) Analysis:** This gives the global perspective of design trade-offs, to make decisions based on application specific priorities.
- **Simulation and Benchmarking:** It simulates the designs through industry standard tools and benchmarks them with the existing solutions to confirm the improvements.

This framework makes sure that the chosen methodologies have materialized returns in the various design objectives[21,22].

4. Discussions

The current low power VLSI design is based on the synergistic use of various complementary circuits, architectural and device design techniques at a circuit, architectural and device level to obtain significant energy savings. Circuit-level techniques like clock gating and multi-threshold CMOS still hold a seminal role: the non-functioning logic is selectively disabled and idle blocks reduced to a minimum leakage. These schemes are robust, familiar, and compatible with normal design flows, a factor that renders them inevitable in both business and research oriented systems. Conversely, more flexible adaptive techniques such as dynamic voltage and frequency scaling and near-threshold computing offer the opportunity to adjust supply parameters to real-time workload demand. This makes systems run well in diverse conditions of performance and greatly minimizes the dynamic power.

On the device level, improved leakage control has been achieved with higher electrostatic conductivity and lower variability, including the FinFET and fully-depleted SOI technology. These innovations enable the designers to retain the performance and reduce operating voltages. Parallel to the above, machine learning has been introduced as a revolutionary power optimization tool. The methods of ML assist predictive modeling, hotspots identification, and automated design-space exploration, which allow the estimation of the power at earlier stages more accurately, and optimizing the design process in a shorter period of time. Together with the current development of fabrication methods, these ML-based methods facilitate the development of robust, ultra-low-power solutions to IoT and biomedical electronics and edge-computing devices. Comparison of all next generation low power methodologies are given in table 1.

Table 1: Comparison of all next generation low power methodologies.

Category	Technique	**Description**	**Power Impact**	**Advantages**	**Limitations**
Circuit-Level	Multi-Threshold CMOS (MTCMOS)	Uses high-Vt and low-Vt transistors to balance speed and leakage	Leakage	Strong leakage reduction	Larger area, increased design complexity
Circuit-Level	Power Gating	Disconnects unused logic blocks using sleep transistors	Leakage	Near-zero standby power	Wake-up delay; area overhead
Circuit-Level	Clock Gating	Disables clock to idle modules to minimize switching	Dynamic	Simple, effective	Cannot reduce leakage
Dynamic Management	DVFS	Dynamically adjusts voltage/frequency per workload	Dynamic + leakage	Large power savings	Requires regulators; design complexity

Dynamic Management	Near-Threshold Computing (NTC)	Operates circuits close to threshold voltage	Dynamic + leakage	Ultra-low power	Large delay variations
Device-Level	TFETs, CNTFETs, NEMS	Novel devices enabling low-voltage or mechanical switching	Dynamic + leakage	Very low leakage; sub-threshold operation	Fabrication and reliability challenges
Architecture-Level	Power Domains / Power Islands	Independently switches power to chip blocks	Dynamic + leakage	Fine-grained control	Requires complex management circuits
Architecture-Level	Resource Sharing & Reconfigurable Logic	Dynamically allocates ALUs, DSPs, memory	Dynamic	High utilization	Reconfiguration cost
Architecture-Level	Memory & Interconnect Optimization	Memory banking, compression, low-power buses	Dynamic	Reduces data-transfer energy	Added control complexity
ML-Driven Optimization	Predictive Modeling	ML predicts power hotspots/design trade-offs	Dynamic + leakage	Faster estimation, fewer iterations	Dataset dependence
ML-Driven Optimization	Reinforcement Learning	RL agent explores design space for optimal configs	Dynamic + leakage	Automates complex tuning	High training cost
ML-Driven Optimization	Clustering & Feature Selection	Detects high-power regions for targeted optimization	Dynamic + leakage	Efficient hotspot detection	Model selection sensitivity
Fabrication-Level	FinFET, GAA, FDSOI	Advanced structures improve channel control	Leakage	Ultra-low leakage	Fabrication cost
Fabrication-Level	3D IC / Advanced Packaging	Vertical stacking reduces interconnect length	Dynamic	Lower communication energy	Thermal issues

5. Conclusion

To sum it up, the current VLSI design that consumes a small amount of power is becoming more and more characterized by the combination of various optimization tools that can be applied at the circuit, architectural, and device levels. The conventional techniques like clock gating and multi-threshold CMOS still represent a robust baseline on leakage and dynamic power saving techniques, whereas adaptive methods such as DVFS and near-threshold computing provide the flexibility needed to operate with an energy efficient manner at varying workloads. Leakage control and scalability is further enhanced by transition to advanced device technologies including FinFET and FDSOI. Meanwhile, machine learning has added a new layer to power optimization and made it possible to predictively model, explore design space automatically, and make better estimations at the earlier design flow phases. These ML-driven methods, combined with advances in the fabrication methods, enable the creation of ultra-low-power systems that can be applied to new designs in the IoT, biomedical interfaces, and edge computing, eventually leading to further optimization of VLSI design.

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