Design of an Active Inductor Based Enhanced CMOS LNA Circuit

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The current state of radio frequency identification (RFID) technology is protocol specific to modern applications. In order to enable tag communication using a single protocol, the reader must either be universal or avoided when using a common RFID standard in Internet of Things (IoT) devices. For 2.4 GHz IoT RFID applications, it is recommended to use a complementary metal oxide semiconductor (CMOS) low noise amplifier (LNA). The limitations associated with spiral inductor-based LNAs, such as their large die area, low Q factor, and limited tuning flexibility, remain unresolved. Consequently, an LNA is developed using an inductor-free approach on a 90nm CMOS process. The post-layout simulation shows a 2.4 GHz bandwidth, 19 dB gain, and 1.55 dB noise figure. The LNA uses a relatively little amount of power from a 1.5 V source is just 1.08 mW. The inductor-less method has allowed for the achievement of an extremely tiny layout measuring 127.7 μm2.

Keywords: Low energy technology, stabilization, LNA, I/O matching

1. Introduction

Currently, the most dependable wireless communication standard for exchanging and storing information is radio frequency identification. RFID communication uses HF to microwave frequencies to exchange information between tags, readers, and information processing units [1]. All things considered, the cost of the reader is nearly equal to the whole cost of the system, which is a barrier to RFID use in internet of things (IoT) devices. Proposing a resolution to this concern, modern IEEE 802.11b protocol-based RFID recommends replacing the RFID reader with wireless network interface cards employing the IPV6 concept [2]. The components of an IoT RFID front-end are illustrated in Figure 1. An LNA, which manages the raw signal that the antenna has intercepted, is regarded as a highly important block. A tank circuit is necessary for an LNA design; however, onchip inductors are not recommended for usage in microwave circuits due to high loss and larger die size. For many fascinating applications, inductors are thought to be essential for the analogue front-end of all radio frequency systems [3–12]. On-chip inductors are typically used in RF regime amplifiers and

filters. However, parasitic losses affect inductors on silicon substrates, which lowers the performance of RF devices. Furthermore, issues such as die size, reduced quality (Q) factor, restricted tuning flexibility, and so forth force designers of radio frequency integrated circuits (RFICs) to consider alternate [6].

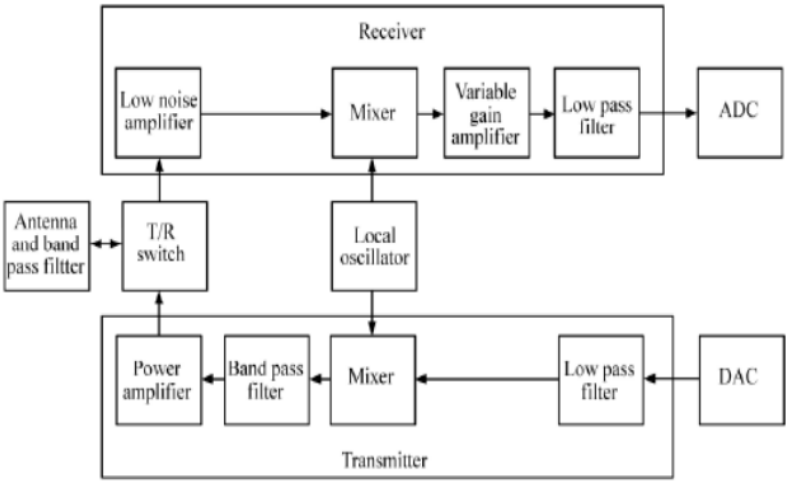

Figure 1 The front-end of IoT RFID.

MOS based active inductors are offered as a solution to overcome the drawbacks. The advantage of correctly adjusting these active inducers is that it can offset the impacts of Process-Voltage-Temperature (PVT) change. Furthermore, in comparison to its on-chip equivalent, they may provide a better quality factor and greater inductance value at just 10% of the die [13]. As such, passive inductors are no longer the first choice of RFIC designers, despite the tremendous developments in integrated circuit technologies.

As seen in Fig. 2, the impression of active inductor which is a result of gyrator model [14, 15]. This circuit has two ports and is made up of two transconductors coupled in a negative feedback loop.

2. Methodology, Result and Discussion:

1 Gbps of data is sent on the 3.1–10.6 GHz Ultra-Wideband (UWB) bandwidth. It uses less electricity because it is connected to a quiet environment. UWB technology is used in low-power, high-data-rate applications such as 5G networks, biomedical transceivers, and sensor nodes. The challenge of LNA design in the UWB range is to retain linear response, impedance matching, high gain, and low noise figure while adhering to stability restrictions.

It has been found that common source based biassing in CMOS-based circuits is capable of meeting the aforementioned conditions.

Device body potential's effect is defined as:

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\emptyset_f| + V_{SB}} - \sqrt{|2\emptyset_f|}\right)$$

V_{TH0}: is the threshold voltage at zero source-bulk potential, and γ is a body-effect parameter, which is a process factor. where ϕf: is the work function of a semiconductor. The CG-CS topologies configured as current reuse are used by the proposed UWBLNA.

The input CG stage aids in matching the input across a broad frequency range. To improve output impedance match and achieve a flat, high power gain, the output CS stage is employed.

A biassing technique is used to maximise the CG stage gain in order to get broader enhanced gain.

The series gate peaking approach is employed to improve the gain of the CG and CS stages, hence improving the LNA gain. The proposed LNA's gain was managed by the use of inductive resistive shunt peaking. The intended LNA gain formula, which takes total transconductance into account, is given by the following equation (g_{mT1}):

$$A = \frac{(1 + g_{mT1} r_{o1}) g_{m2} ((R_{d2} + j\omega L_{d2}) // R_{out})}{(r_{o1} + j\omega L_{d1}) j\omega C_{gs2}}$$

By employing this biasing technique, the input-referred components of gate thermal and flicker noise are minimized, while maximizing the device transconductance [1].

Furthermore, an inter-stage LC matching network is utilized to enhance noise immunity and improve performance [2].

The parallel inductor peaking approach is used to adopt a good value of output corresponding for output return loss. The inductive resistive network's controlling quality factor determines the stages matching bandwidth. Furthermore, in order to increase the output impedance matching's bandwidth, a resistive termination with a parallel output resistance was included at the output in the suggested design.

3. Conventional LNA design:

The LNA is modelled and designed using 130nm CMOS technology.

Gain in Power and Noise Level The intended range from 3.1 GHz to 10.6 GHz is covered by the 9.75±2.75 dB gain of the planned LNA. Techniques like FBB and inductive peaking are responsible for this increase in power gain.

Figure 2 displays the results of the LNA achieved gain simulation. The outcomes of the pre- and post-layout simulations are compared. Fig. 3 displays the post-layout results compared to the prelayout results of NF. The minimal post-layout noise figure of this very low-power LNA is 3.9 dB. The bulk conductance's presence boosts this LNA increase without requiring excessive power usage. To achieve forward biassing, the bulk potential is adjusted to have zero passing current in the bulk. In order to properly utilise biassing, a series resistive (Rb) current blocking was included to assure lower scrounging losses and prevent power indulgence in bulk.

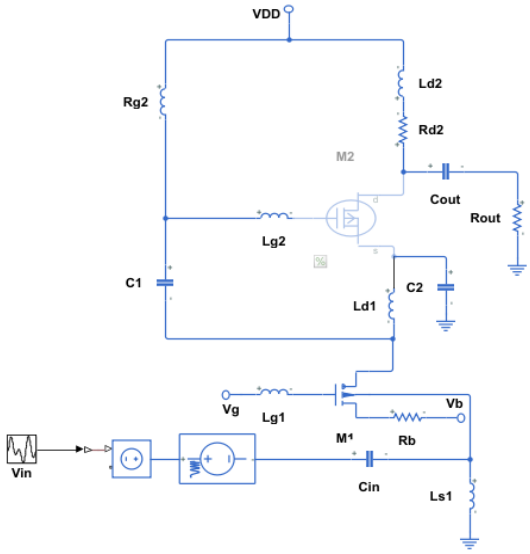

Figure 2 Conventional LNA circuit design

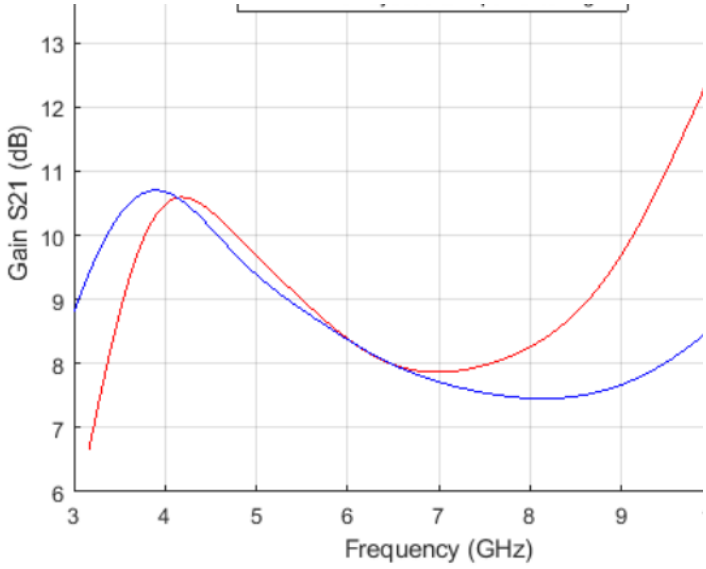

Figure 3 Gain vs frequency plot for Conventional LNA

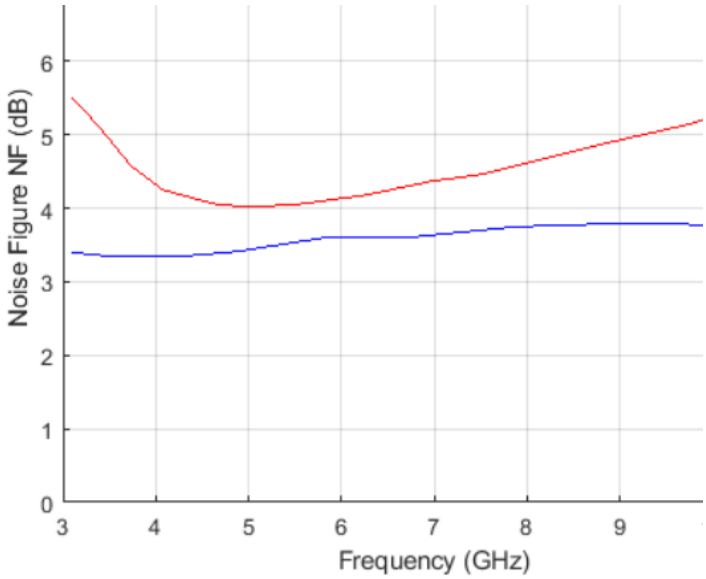

Figure 4 Noise Figure vs frequency plot for Conventional LNA

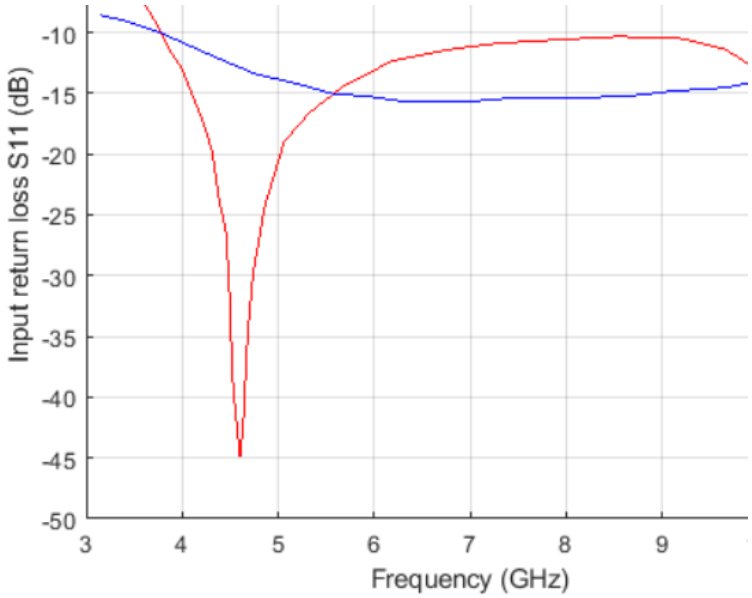

Figure 5 Input return loss vs frequency plot for Conventional LNA

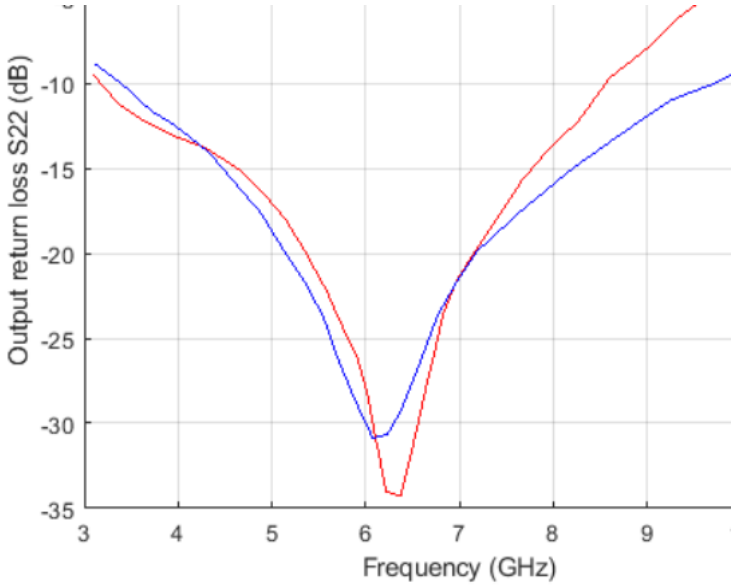

Figure 6 Output return loss vs frequency plot for Conventional LNA

4. LNA Design Proposed

In microwave circuits, on-chip inductors are not recommended due to increased loss and bigger die size; nonetheless, an LNA circuit requires a tank circuit.

The performance of RF devices is lowered by parasitic losses inductors in silicon substrates.

MOS based active inductors are offered as a solution to overcome the drawbacks.

The gyrator model has an impact on how the active inductor is perceived.

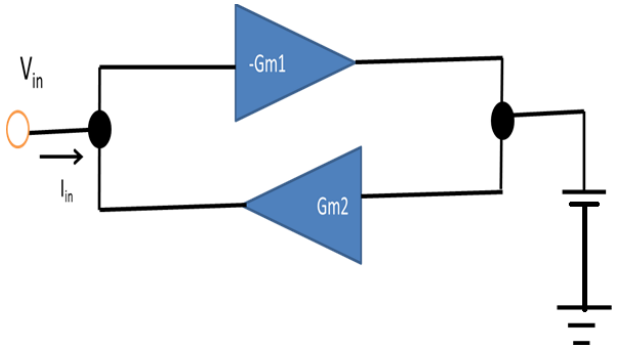

Figure 7 The perception of a gyrator.

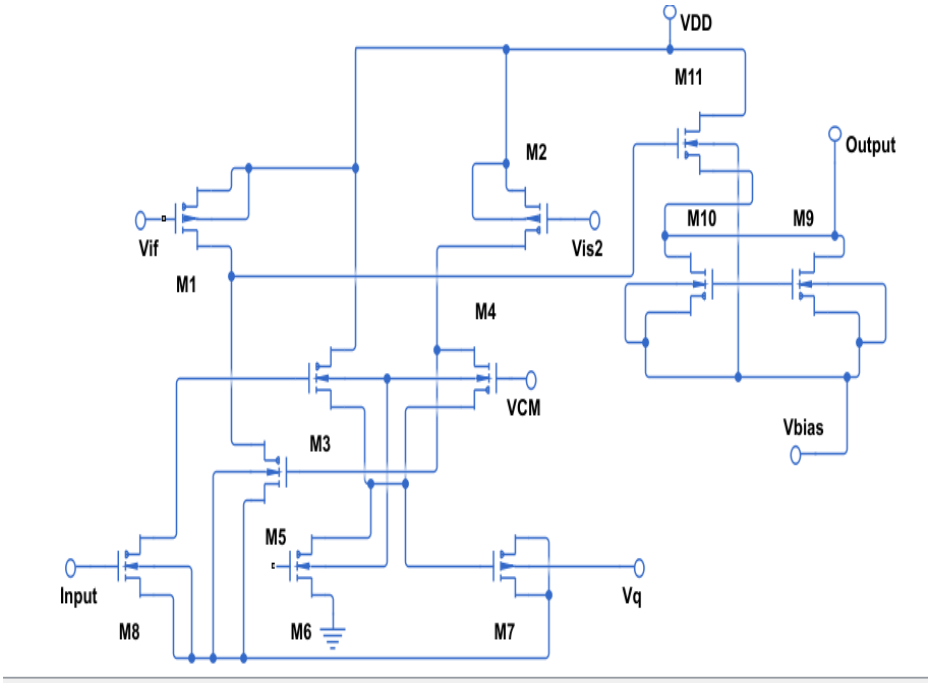

Figure 8 Proposed LNA circuit design

- LNA schematic:
- M1, M3, M4 (10/0.36),
- M2 (30/0.36),
- M5, M6 (3/0.36), M7, M8, M9 10 (0.12/0.36), M11 (1/0.36),
- VIF, Vis/2,
- Vis = 0.85V,
- Vq = 0.7V,
- Vcm = 0.7V,
- VDD = 1.5V.

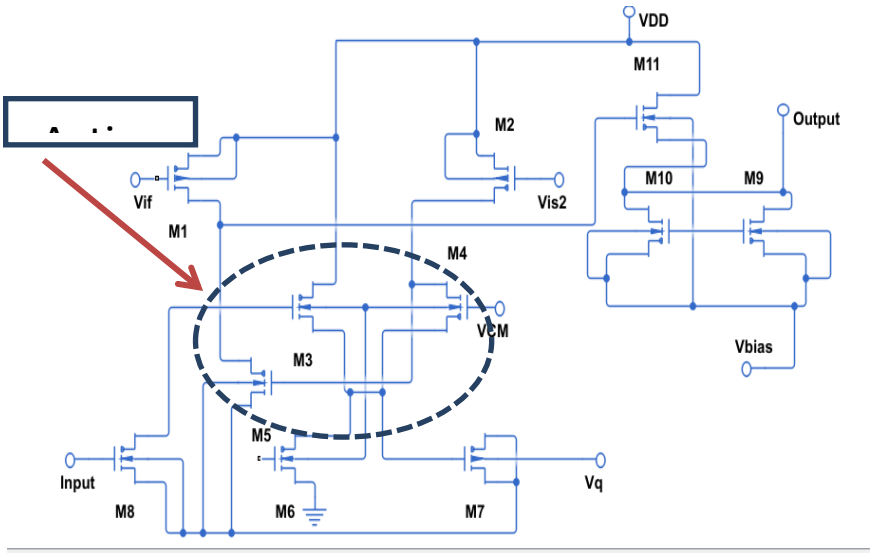

Figure 9 Location of active inductor in proposed LNA design.

The very low admittance at the resonance frequency of an active inductor makes it possible to use it as a tank circuit. The active inductor circuit schematic for the suggested LNA is shown in Fig. In this instance, the non-inverting transconductor (GM1) represented by M3 and M4 has an input voltage of V1 and an output current of V3. M5, an inverting transconductor (–GM2), has an output current of V1 and an input voltage of V3. The gyrator core is made up of these two transconductances. At node 3, the parasitic capacitor C1 and the gyrator combine to form an active inductor. Through analysis of the inductor equivalent depicted in the figure, the component values are determined:

$$L_{eq} = \frac{GC_3}{g_{m1}g_{m2}g_{m3}} \approx \frac{C_3}{0.5g_{m1}g_{m3}}$$

$$r_{loss} = \frac{g_3}{0.5g_{m1}g_{m3}}$$

$$C_p = C_1$$

$$R_p = \frac{1}{g_1}$$

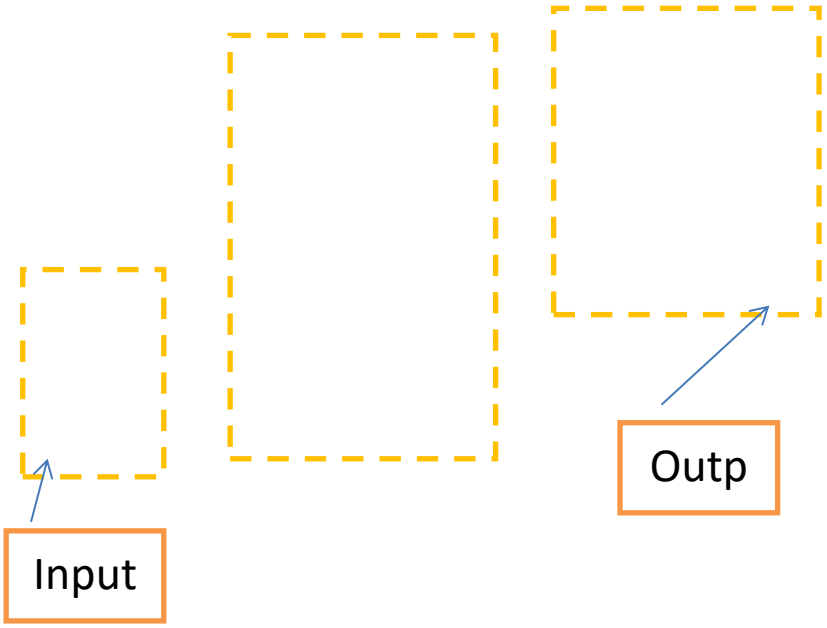

Figure 10 Position of stages in proposed LNA circuit with input buffer active inductor and output buffer

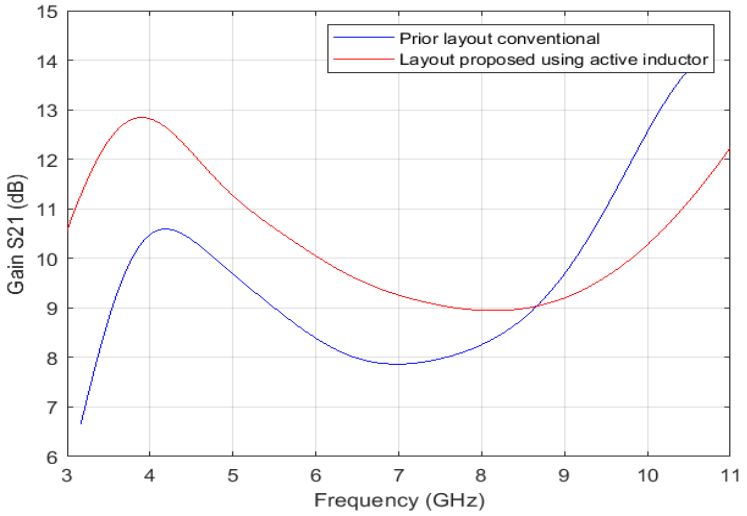

Figure 11 Comparison of gain versus frequency plots for both Conventional and proposed Low-Noise Amplifiers (LNAs).

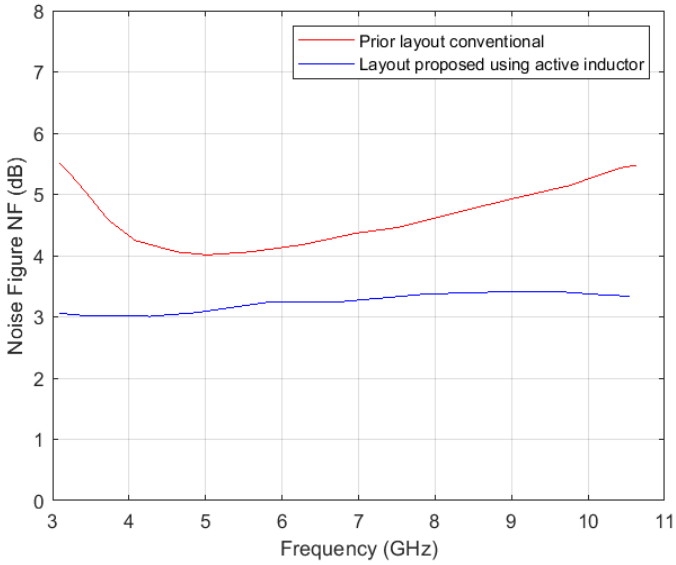

Figure 12 Noise figure vs frequency plot for Conventional and proposed LNA

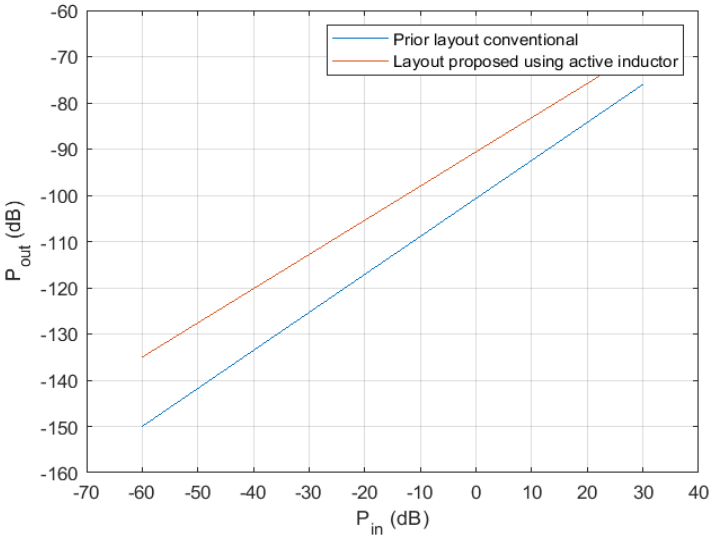

Figure 13 Pout vs Pin plot for Conventional and proposed LNA

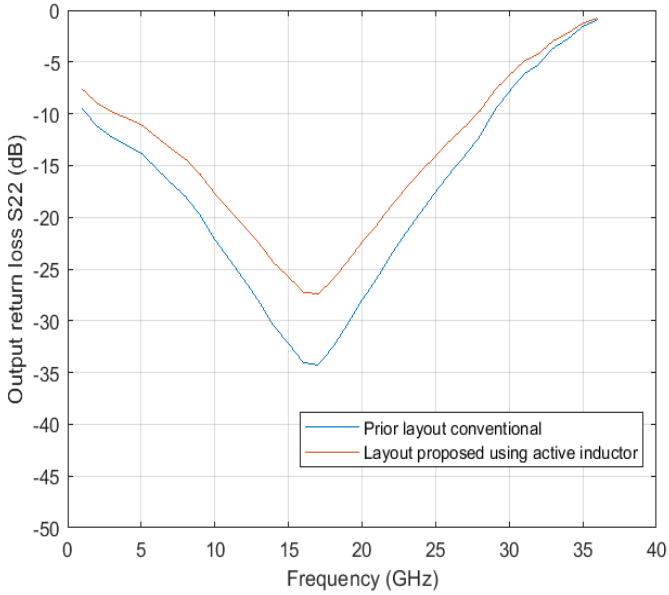

Figure 14 Output return loss vs frequency plot for Conventional and proposed LNA

5. Conclusion:

1 Gbps of data is sent on the 3.1–10.6 GHz Ultra-Wideband (UWB) bandwidth. It uses less electricity because it is connected to a quiet environment. UWB technology is used in low-power, high-data-rate applications such as 5G networks, biomedical transceivers, and sensor nodes. The challenge of LNA design in the UWB range is to retain linear response, impedance matching, high gain, and low noise figure while adhering to stability restrictions. It is found that CMOS-based circuits with active inductors can meet the aforementioned requirements.

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